Hardware Design Guide

for efus™ backplane

Version 1.01
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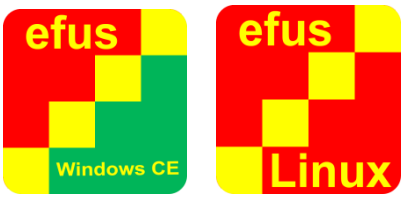

Elektronik Systeme

Untere Waldplätze 23
D-70569 Stuttgart
Fon: +49(0)711-123722-0
Fax: +49(0)711-123722-99

About This Document

This document describes how to design an efus baseboard. The latest version of this document can be found at:

http://www.fs-net.de

History

Date	V	Platform	A,M,R	Chapter	Description	Au
2014-05-22	0.1	All	A	-	Build the document	KW
2014-07-01	0,2	All	M	*	Changed to new company CI	JG
2015-08-05	0.3	All	M	4	Change USB_DEV_PWR_Onn to low active (pin 219)	KW
2016-06-28	0.4	All	M		Change 3.1 Fixing the modul	MW
2017-10-16	0.5	All	A	3.2, 3.3	Add new information for plastic latch	KW
2017-10-17	1.0	All	A		Add RGB connection details	KW
2010-04-15	1.01	All	M	5.2	Change differential impdance from 95 to 100Ohm	DB

V	Version
A,M,R	Added, Modified, Removed
Au	Author

Table of Contents

1 Introduction

The efus form factor was created by F&S Elektronik Systeme GmbH by congregate 20 years of ARM knowledge and experience. With other form factors we always missed some functions or have a larger size.

Just a quick comparison:

	Qseven®	SMARC®	nanoRISC®	efus®
GBitE	1x	1x	1x (or 2x 10/100Mbit)	2x (just 1x or 2x 100Mbit on some modules)
USB Host	Up to 6x often 4x from Hub	3x (1x out from CPU to USB Hub on module)	1x	1x out from CPU (use Quad-USB Hub on your base board to get 4x)
USB Client	1x	1x	1x	1x
LVDS	2x LVDS 24Bit via goldfinger	2x LVDS 24Bit via goldfinger	None	2x LVDS 24Bit connector on module
Digital RGB	none	24 Bit	24 Bit	18 Bit
DVI/DP	1	1	None	1
Camera	none	CSI or parallel	Parallel	CSI or parallel
SDIO	2x	1x	1x (+1x on module)	2x
PCIe	1x	3x (often 1x im-plemented)	None	1x
RS232	2x	4x	2x	4x (2x RX/TX, 2x RX/TX/CTS/RTS)
I2C	2x, 1 dedicated IRQ	4x	2x	2x, dedicated IRQs
SPI	1x	2x	2x	2x, dedicated IRQs
CAN	1x	2x	2x	2x
GPIO's	0	Up to 12 by using SD card signals	53, some are IRQs	Up to 85 by using SD card, UART, SPI, I2C, LCD RGB signals
LPC	up to 1 (only available on x86)	none	none	none
Size	70x70 4900 mm^2	82x50 4100 mm^2	70x50 3500 mm^2	62.12x47 2920 mm^2

The efus design guide is been created to help customer to design an efus compatible baseboard. Our engineers are sharing their expertise to reduce problems by schematic and layout. Any suggestion for additional information and any feedback about the content are welcome. Please contact support@fs-net.de for your feedback.

For designing your own base board you can use our example Layout created with CadSoft EAGLE® V6 which you can get on our homepage http://www.fs-net.de.

This includes a lot of schematic and layout symbols to make the baseboard design easy.

We strictly recommend Eagle Version ≥6 because the needed differential routing feature.

1.1 Design Review

We recommend to send us your schematic (Eagle format or searchable PDF), your layout (Eagle or Gerber) and the impedance calculation for a review. So we can check your work with our knowledge to avoid some later problems.

Please contact support@fs-net.de doing this.

2 Mechanical dimension

The efus module is a 230 pin edge finger module using MXM-2 connector.

The smallest possible module is 62.12x47mm

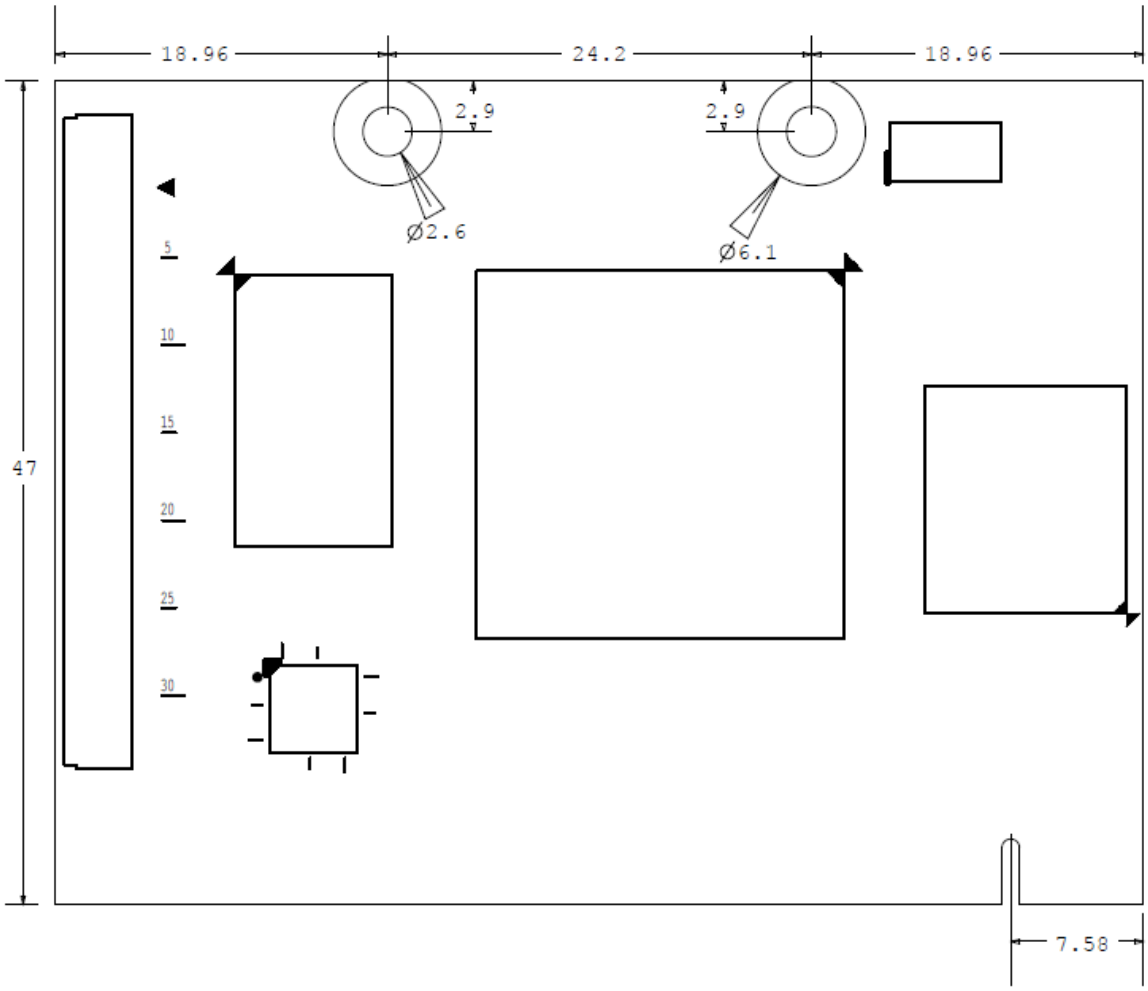

Figure 1: mechanical dimension

To extend functionality of this COM with additional functions like WLAN, Bluetooth and wireless smart home modules with a 20mm extended area are in planning.

This will extend the board size to 82.12x47mm.

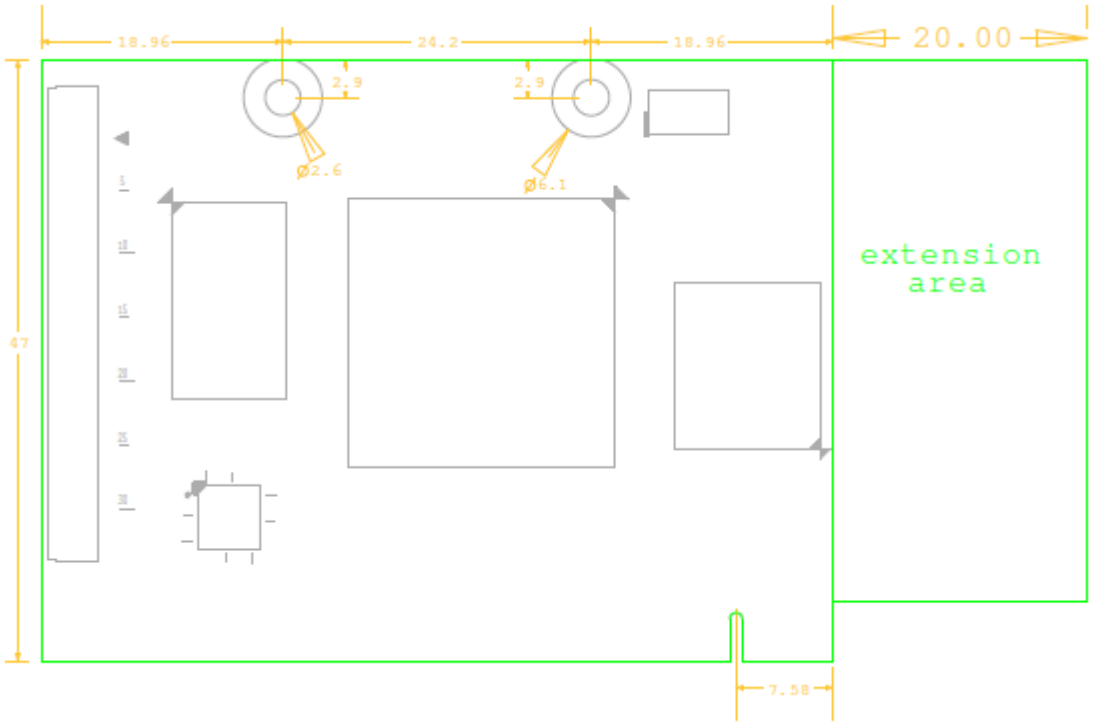

Figure 2: mechanical dimension with extension area

3 MXM connector

Manufacturer	Order Number	Height between carrier and efus module
Foxconn	AS0B326-S78N-7F	5.0mm (phased out from manufacturer)
Aces	88882-2D0K	5.0mm
Taitek	106020BE75A	5.0mm
Yamaichi (*)	BEC-0.5-230-S9-FF-R-EDC	5.0mm
Foxconn	AS0B326-S55N-7F	2.7mm (phased out from manufacturer)
Aces	88885-2D0T	2.7mm

(*) Yamaichi connector is made for requirements for the automotive industry and needs a different layout shape.

We always recommend qualifying all fitting connectors on your baseboard to have second source in case of allocation or EOL.

The shape for the layout differs between manufacturers, especially the size of the mounting flap. Please recheck this in your layout.

3.1 Fixing the Modul

To fix the efus-Module we recommend using 2.5mm distance bolts.

By using distance bolts they should match the board to board height with a maximum outer diameter 6mm.

3.2 MXM connector layout footprint

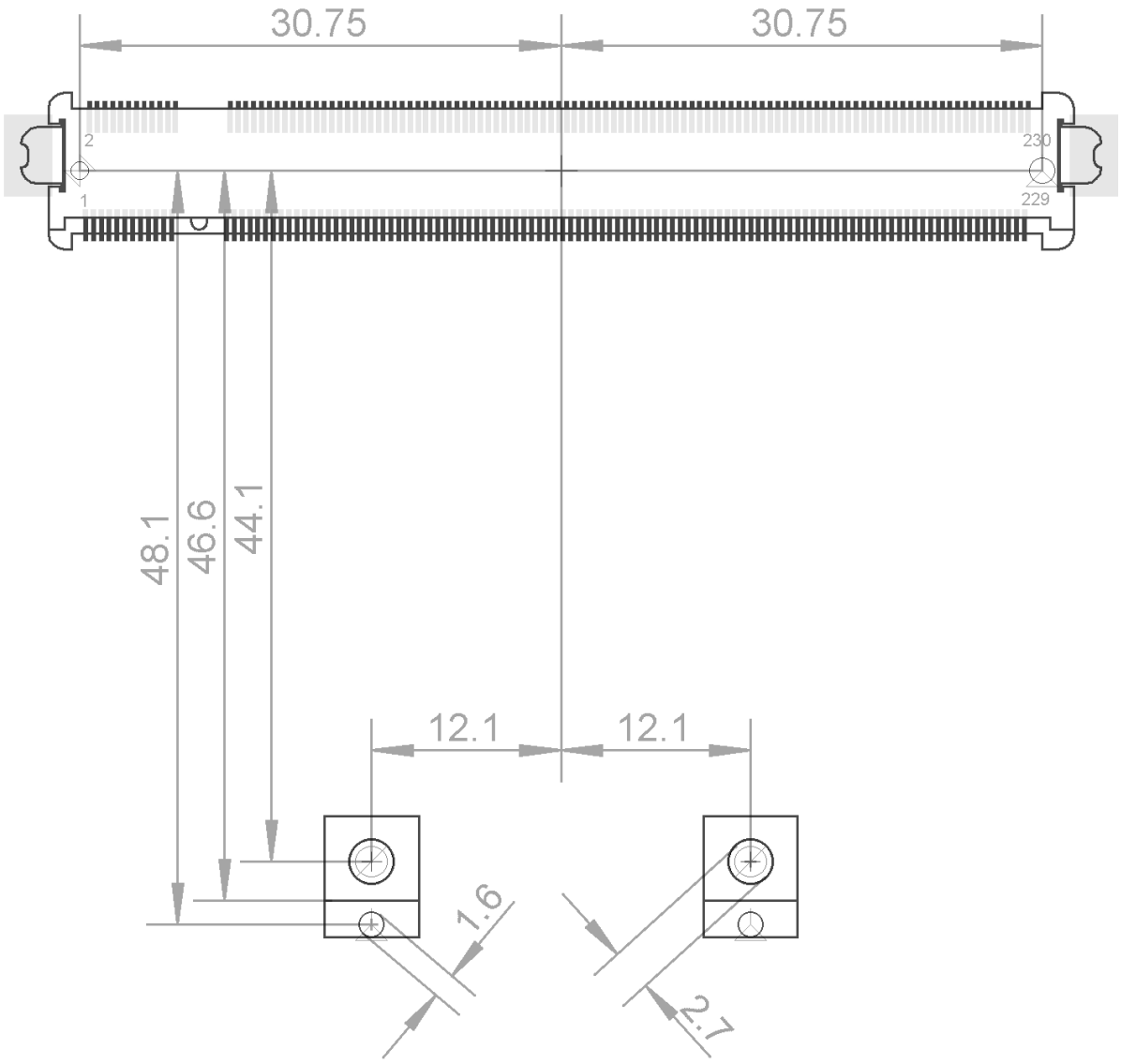

Figure 3: connector and mounting holes layout footprint

Midpoint of 2.7mm will match with the efus mounting holes. Please correct diameter for your spacer.

Additional 1.6mm hole is needed by using the plastic efus latches from F&S.

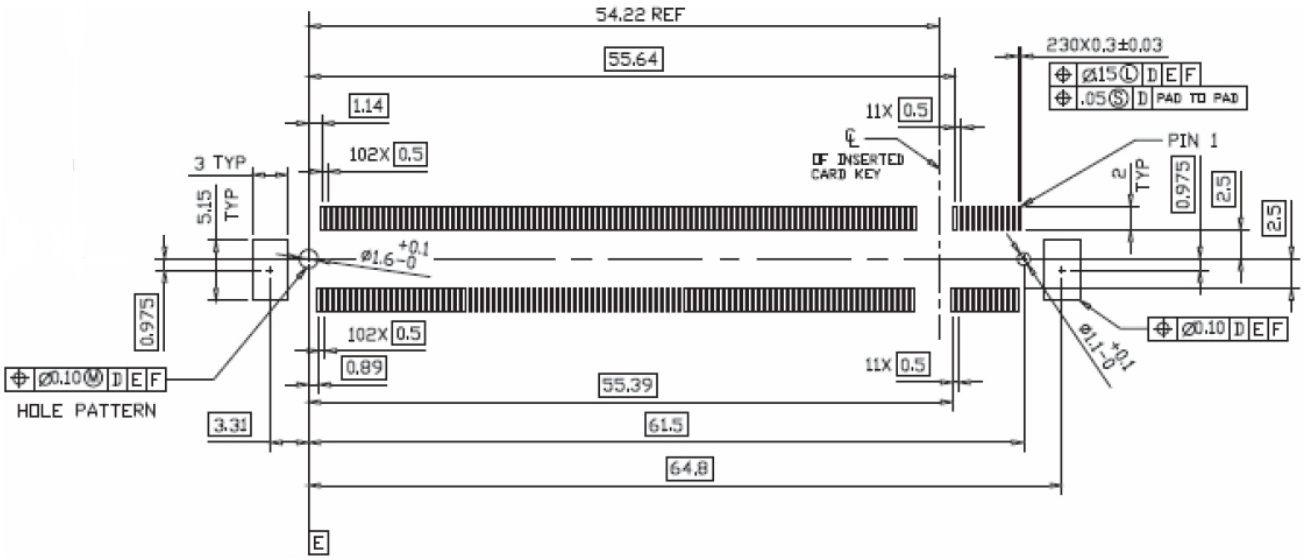

Figure 4: connector layout footprint detail

3.3 Plastic efus mounting latch

For easy mounting F&S does provide plastic latches (called “efus latch clip-on” from F&S sales).

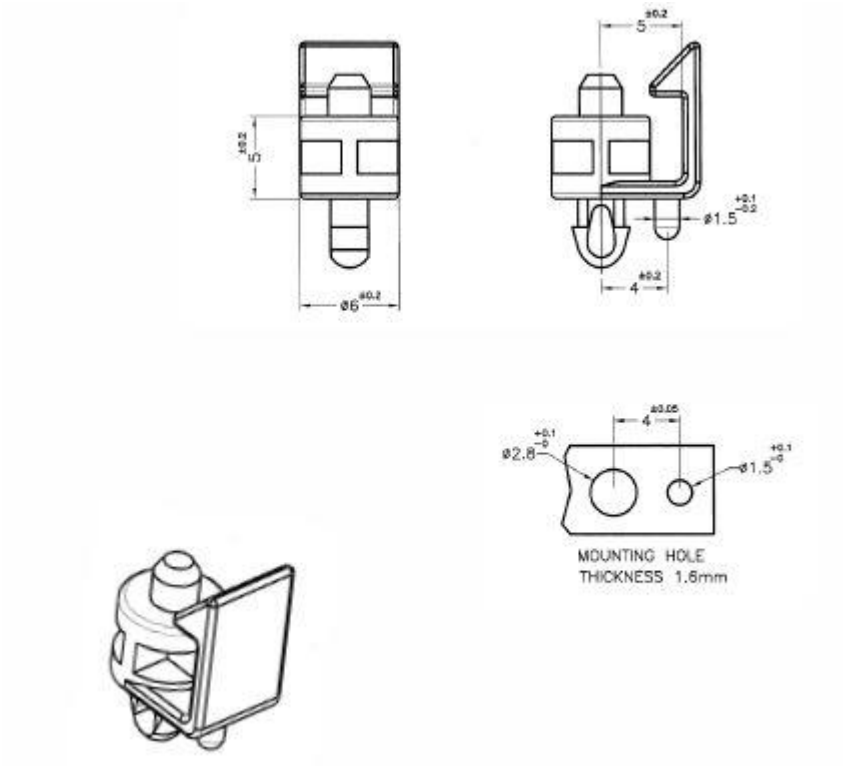

Figure 5: efus clip measurement detail

This clip is designed for baseboard PCB thickness between 1.5 and 1.65mm and for MXM connector height 5mm.

4 Pin assignment

The efus module is plugged on this connector.

Pin	Default function	Description	marks
1	+5V Power In	5V ±5% Power input Connector limit is 3A. Please refer module datasheet for maximum supply current.	
2	+5V Power In		
3	+5V Power In		
4	+5V Power In		
5	+5V Power In		
6	+5V Power In		
7	GND		
8	GND		
9	VBAT In	RTC battery input 2.8 … 3.45V	
10	V33-Enable	EN output for baseboard DCDC switcher. 3.3V VOUT with limited current ≥50mA. Please refer module datasheet.	
11	ACOK	USB Charger detect signal (for future use)	
12	!RESET_IN	Drive with OC/OD, 3.3V PU on module	
13	IOOUT_ADC_IN	Battery monitoring pin (for future use)	*1
14	!RESET_OUT	Low active reset for baseboard logic; Controlled by GPIO, 4.7kΩ PD on module	
15	RXD_C_TTL	UARTC RX in	# *2
16	SD_A_WP	SDIO A write protect input	# *1 *2
17	TXD_C_TTL	UARTC TX out	# *2
18	SD_A_CD	SDIO A card detect input	# *1 *2
19	RTS_C_TTL	UARTC RTS out	# *2
20	SD_A_DAT2	SDIO A data 2	# *1 *2
21	CTS_C_TTL	UARTC CTS in	# *2
22	SD_A_DAT3	SDIO A data 3	# *1 *2
23	PWM_B	Universial PWM output; functionality could different between different boards	# *1
24	SD_A_CMD	SDIO A command	# *1 *2
25	PWM_A	Universal PWM output; functionality could different between different boards	# *1

Pin	Default function	Description	marks
26	SD_A_VCC	SDIO A VCC output	# *1 *2
27	GND		
28	SD_A_CLK	SDIO A clock	
29	CAN_A_TX	CAN A TX out	
30	GND		
31	CAN_A_RX	CAN A RX in	
32	SD_A_DAT0	SDIO A data 0	# *1 *2
33	GND		
34	SD_A_DAT1	SDIO A data 1	# *1 *2
35	CAN_B_TX	CAN B TX out	# *1
36	RESERVED1		
37	CAN_B_RX	CAN B RX in	# *1
38	RESERVED2		
39	GND		
40	RESERVED3		
41	MPCIE_CTX_P	PCIe differential TX+	*1
42	RESERVED4		
43	MPCIE_CTX_N	PCIe differential TX-	*1
44	RESERVED5		
45	GND		
46	GND		
47	MPCIE_CRX_P	PCIe differential RX+	*1
48	EXT_PROG	For Manufacturing and restore only; could have different function from board to board	
49	MPCIE_CRX_N	PCIe differential RX-	*1
50	SPI_B_MISO	SPI B Master In Slave Out	# *1
51	GND		
52	SPI_B_MOSI	SPI B Master Out Slave In	# *1
53	MPCIE_CLK_P	PCIe differential CLK+	*1
54	SPI_B_SPCK	SPI B Clock	# *1
55	MPCIE_CLK_N	PCIe differential CLK-	*1
56	SPI_B_CS1	SPI B 1st Chip Select	# *1

Pin	Default function	Description	marks
57	GND		
58	SPI_B_CS2	SPI B 2nd Chip Select	# *1
59	MPCIE_PERST	PCIe Reset out	*1
60	SPI_B_IRQ1	SPI B 1st IRQ input	# *1
61	MPCIE_WAKE	PCIe wake signal	*1
62	SPI_B_IRQ2	SPI B 2nd IRQ input	# *1
63	GND		
64	GND		
65	SD_B_DAT2	SDIO B data 2	#
66	SPI_A_MISO	SPI A Master In Slave Out	#
67	SD_B_DAT3	SDIO B data 3	#
68	SPI_A_MOSI	SPI A Master Out Slave In	#
69	SD_B_CMD	SDIO B command	#
70	SPI_A_SPCK	SPI A clock	#
71	SD_B_VCC	SDIO B VCC output	
72	SPI_A_CS1	SPI A 1st Chip Select	#
73	SD_B_CLK	SDIO B clock	#
74	SPI_A_CS2	SPI A 2nd chip select	#
75	GND		
76	SPI_A_IRQ1	SPI A 1st IRQ input	#
77	SD_B_DAT0	SDIO B data 0	#
78	SPI_A_IRQ2	SPI A 2nd IRQ input	#
79	SD_B_DAT1	SDIO B data 1	#
80	GND		
81	SD_B_WP	SDIO B write protect input	#
82	I2C_B_DAT	I2C B data, PU on module	#
83	SD_B_CD	SDIO B card detect input	#
84	I2C_B_CLK	I2C B clock, PU on module	#
85	GND		
86	I2C_B_IRQ	I2C B IRQ input, PU on module	#
87	BL_CTRL	PWM Backlight dimming	
88	I2C_B_RST	I2C B Reset output	

Pin	Default function	Description	marks
89	VBL_ON	Backlight on	
90	GND		
91	GND		
92	RXD_A_TTL	UART A RX input, debug port	
93	LCD_CLK	LCD clock output	#
94	TXD_A_TTL	UART A TX output, debug port	
95	GND		
96	RXD_D_TTL	UART D RX input	#
97	LCD_HSYNC	LCD HSYNC	#
98	TXD_D_TTL	UART D TX output	#
99	LCD_VSYNC	LCD VSYNC	#
100	GND		
101	GND		
102	RXD_B_TTL	UART B RX input	#
103	LCD_R0	LCD red 0	#
104	TXD_B_TTL	UART B TX output	#
105	LCD_R1	LCD red 1	#
106	RTS_B_TTL	UART B RTS output	#
107	LCD_R2	LCD red 2	#
108	CTS_B_TTL	UART B CTS input	#
109	LCD_R3	LCD red 3	#
110	GND		
111	LCD_R4	LCD red 4	#
112	I2S_MCLK	Audio I2S MCLK	#
113	LCD_R5	LCD red 5	#
114	GND		
115	GND		
116	I2S_LRCLK	Audio I2S LRCLK	#
117	LCD_G0	LCD green 0	#
118	GND		
119	LCD_G1	LCD green 1	#
120	I2S_SCLK	Audio I2S SCLK	#

Pin	Default function	Description	marks
121	LCD_G2	LCD green 2	#
122	GND		
123	LCD_G3	LCD green 3	#
124	I2S_DOUT	Audio I2S data out	#
125	LCD_G4	LCD green 4	#
126	I2S_DIN	Audio I2S data in	#
127	LCD_G5	LCD green 5	#
128	GND		
129	GND		
130	I2C_C_DAT	I2C C data, PU on module, shared with functionality on module, recommended for I2S codec, SMB, camera, DDC	
131	LCD_B0	LCD blue 0	#
132	I2C_C_CLK	I2C C clock, PU on module, shared with functionality on module, recommended for I2S codec, SMB, camera, DDC	
133	LCD_B1	LCD blue 1	#
134	DVI_DDC_VOUT	3.3V output for DVI ESD protection	
135	LCD_B2	LCD blue 2	#
136	GND		
137	LCD_B3	LCD blue 3	#
138	DVI_DATA2_P	Differential DVI data2+	*4
139	LCD_B4	LCD blue 4	#
140	DVI_DATA2_N	Differential DVI data2-	*4
141	LCD_B5	LCD blue 5	#
142	DVI_DATA1_P	Differential DVI data1+	*4
143	GND		
144	DVI_DATA1_N	Differential DVI data1-	*4
145	LCD_DE	LCD DE	
146	DVI_DATA0_P	Differential DVI data0+	*4
147	GND		
148	DVI_DATA0_N	Differential DVI data0-	*4
149	VLCD_ON	LCD power on output	
150	DVI_CLK_P	Differential DVI clock+	*4
151	I2C_A_DAT	I2C A data	#

Pin	Default function	Description	marks
152	DVI_CLK_N	Differential DVI clock-	*4
153	I2C_A_IRQ	I2C A interrupt input	#
154	GND		*4
155	I2C_A_CLK	I2C A clock	#
156	DVI_DDCCEC	DVI CEC serial bus	*4
157	I2C_A_RST	I2C A reset output	#
158	DVI_HPD	DVI hotplug detect	
159	GND		
160	GND		
161	CAM_D0_N	Differential MIPI CSI camera data0-	
162	ETH_B_D4_N	Differential LAN B data4-	
163	CAM_D0_P	Differential MIPI CSI camera data0+	
164	ETH_B_D4_P	Differential LAN B data4+	
165	CAM_D1_N	Differential MIPI CSI camera data1-	*3
166	ETH_B_LED_ACT	LAN B Activity LED cathode output serial resistor required on baseboard	
167	CAM_D1_P	Differential MIPI CSI camera data1+	*3
168	ETH_B_D3_N	Differential LAN B data3-	
169	CAM_D2_N	Differential MIPI CSI camera data2-	*3
170	ETH_B_D3_P	Differential LAN B data3+	
171	CAM_D2_P	Differential MIPI CSI camera data2+	*3
172	GND		
173	CAM_D3_N	Differential MIPI CSI camera data3-	*3
174	ETH_B_D2_N	Differential LAN B data2-	
175	CAM_D3_P	Differential MIPI CSI camera data3+	*3
176	ETH_B_D2_P	Differential LAN B data2+	
177	CAM_CLK_N	Differential MIPI CSI camera clock-	*3
178	ETH_B_LED_LINK	LAN B Link LED cathode output serial resistor required on baseboard	
179	CAM_CLK_P	Differential MIPI CSI camera clock+	*3
180	ETH_B_D1_N	Differential LAN B data1-	
181	GND		
182	ETH_B_D1_P	Differential LAN B data1+	

Pin	Default function	Description	marks
183	CAM_MCLK	MIPI CSI camera MCLK	*3
184	GND		
185	GND		
186	ETH_CTREF	LAN common transformer pin	
187	reserved		*3
188	ETH_A_D4_N	Differential LAN A data4-	
189	CAM_VCAM	Camera VCC output (3.3V); Could be different in custom version	*3
190	ETH_A_D4_P	Differential LAN A data4+	
191	reserved		*3
192	ETH_A_LED_ACT	LAN A Activity LED cathode output serial resistor required on baseboard	
193	CAM_PWDN	Camera power down output	
194	ETH_A_D3_N	Differential LAN A data3-	
195	reserved		*3
196	ETH_A_D3_P	Differential LAN A data3+	
197	I2C_C_RST	I2C reset out	
198	ETH_A_VLEDOUT	VOUT for common LAN LEDs anode serial resistor required on baseboard	
199	GND		
200	ETH_A_D2_N	Differential LAN A data2-	
201	SATA_RX_P	Differential SATA RX+	
202	ETH_A_D2_P	Differential LAN A data2+	
203	SATA_RX_N	Differential SATA RX-	
204	ETH_A_LED_LINK	LAN A Link LED cathode output serial resistor required on baseboard	
205	SATA_TX_N	Differential SATA TX-	
206	ETH_A_D1_N	Differential LAN a data1-	
207	SATA_TX_P	Differential SATA TX+	
208	ETH_A_D1_P	Differential LAN a data1+	
209	GND		
210	GND		
211	CAM_A_IN	Analog Camera input	*1
212	USB_A_PWRON	USB Host power on output	

Pin	Default function	Description	marks
213	CAM_A_GND	Analog Camera Ground	*1
214	USB_A_N	Differential USB Host-	
215	GND		
216	USB_A_P	Differential USB Host+	
217	USB_DEV_VBUS	USB device VBUS in	
218	GND		
219	USB_DEV_PWR_ONn	USB device power on output, low active	
220	USB_A_SSRX_N	Reserved for USB 3.0	*1
221	USB_DEV_OC	USB device overcurrent input	
222	USB_A_SSRX_P	Reserved for USB 3.0	*1
223	USB_DEV_ID	USB device ID input	
224	GND		
225	USB_DEV_N	Differential USB device-	
226	USB_A_SSTX_N	Reserved for USB 3.0	*1
227	USB_DEV_P	Differential USB device+	
228	USB_A_SSTX_P	Reserved for USB 3.0	*1
229	GND		
230	GND		

GPIO capability, if available on module. Please add weak pull-up to 3.3V (~100kΩ) to avoid floating on Reset and initialization. Never use pull-down (use inverter instead).

*1 function could be missed depends CPU functionality

*2 function could be missed on boards with wireless extension

*3 different function for digital RGB camera interface in customized version

*4 different function for boards supporting DisplayPort instead DVI, will be defined in a future version

5 Layout rules

The efus evaluation board is made on 4 layer FR4 PCB.

As general rule for high speed signals use 55Ω ±15% signal impedance over a GND/ VCC plane.

For right routing you need the layer stackup from your PCB manufacturer and a calculator like the toolkit from http://www.saturnpcb.com/

This is the 4 layer evaluation board stackup

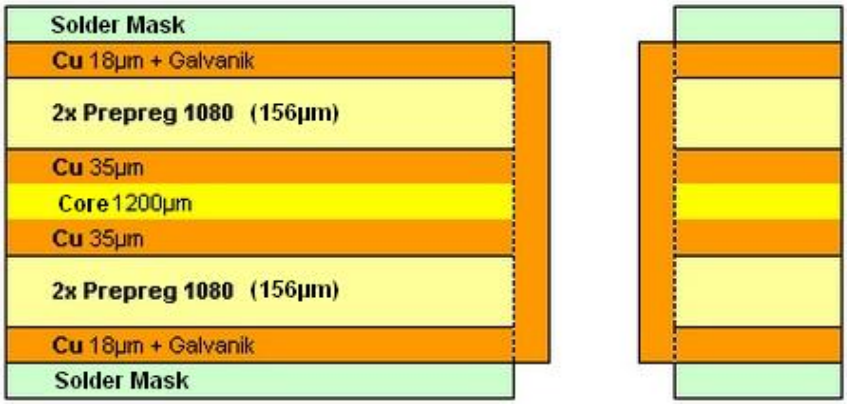

Figure 6: PCB stackup

5.1 Layout rules high-speed signals

High-speed traces should never cross plane split. The distance to anti etch and PCB etch should be ≥25mil (635µm).

Any stub and via does reduce signal quality and will increase EMI.

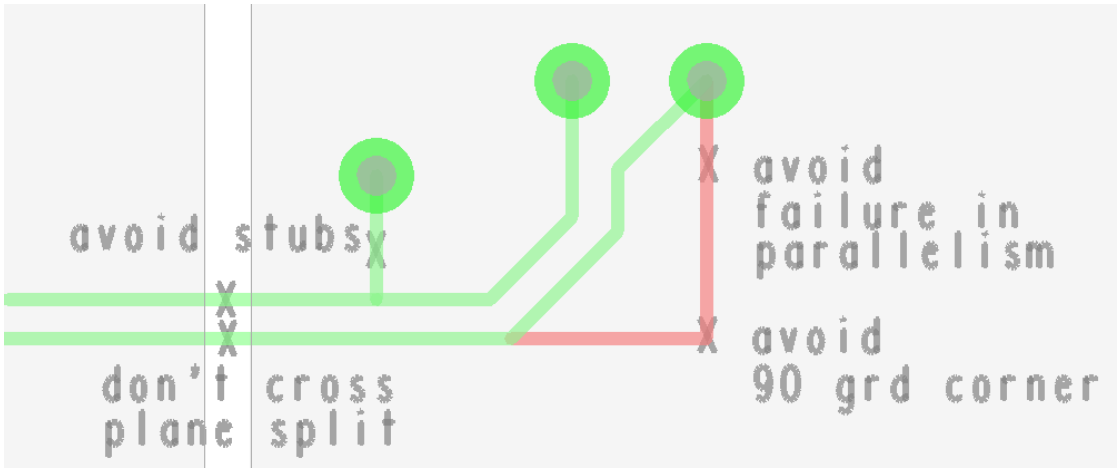

Figure 7: layout rules

We got the following rules for the TOP and BOTTOM signal layer on the evaluation board stackup:

Signals	Z0	Microstrip Trace width
RGB, Audio I2S, SDIO, UART, HS-SPI, CAN	55Ω ±15%	190µm 7.5mil

5.2 Layout rules differential signals

Differential signals should routed as impedance controlled signal.

Signals	Z0	Differential impedance
USB	55Ω ±15%	90Ω ±20%
SATA, LAN, mPCIe, MIPI-CSI, DVI, eDP	55Ω ±15%	100Ω ±20%

The distance to other differential pairs and low speed signals should be ≥500µm.

The distance to high speed signals should be ≥1270µm.

5.3 Layout rules analog signals

Some efus modules does support a analog camera input.

These signals are very sensitive for the noise of digital signals.

So we recommend a large distance (>2mm) to any digital signal.

The separate analog Ground signal should be used for the analog signal. We don't recommend connecting this to the noisy digital GND on the baseboard.

If an external camera connector is used, EMV protection should be connected from analog camera input and analog camera ground to the shield ground. Under the transformer the GND plane should be split in Signal Ground and Shield Ground.

5.4 Rules for Gbit Ethernet

We recommend using a RJ45 connector with integrated transformer. Tested types are listed on the BOM of the evaluation board. The differential pair length between MXM connector and transformer/ connector with transformer should be at least 1 inch (24,5mm) and less than 4 inch (101,6mm). The skew on the same pair should be less than 20mil (0,5mm). To minimize crosstalk, the space between pairs should be 40mil (1mm) or more.

By using a separate transformer the trace length between transformer and RJ45 should be-tween 1,2-2inch (40-50mm)

100-120 mil (2,5-3 mm)

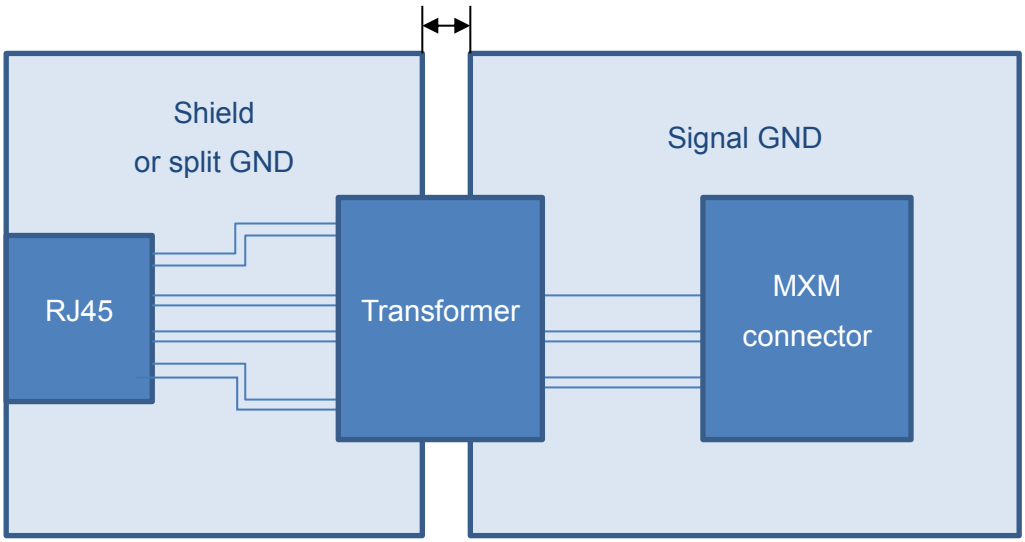

Figure 9: Ethernet transformer plane split

Under the transformer the ground plane should be split. There shouldn't be another plane (VCC) on connector side.

Transformer should be a 1:1 Gbit transformer. A integrated common mode choke on line side of the transformer will reduce EMI.

5.5 Rules for USB

We recommend the "High Speed USB Platform Design Guidelines" from usb.org with highly recommended information for a proper working USB design.

5.6 Rules for PCIe

The maximum length of each pair should not exceed 12" (300mm). The pair to pair spacing should be >20 mil (0,5 mm) to minimize crosstalk.

A good design guide for routing PCIe signals is available from NXP as application note AN307.

6 Rules for power up sequencing

VBAT — For RTC only the module needs a battery with 2.8-3.45V output. We recommend 3V Lithium battery.
If RTC is not used we recommend to leave open this pin.

+5V — The module is working with a single 5V voltage. Max. tolerance is ±5%

+3.3V — The module delivers a small amount of on-board 3.3V for external logic. Depending from the module it could be 50mA or more. Use this voltage as enable for all other regulators on baseboard to avoid backdrive current.

+VLCD — The module can drive ≥500mA switched VLCD on the LVDS connector. Depend the module the available current could be higher; please refer module datasheet.
For displays with higher power consumption or other voltages we recommend to use a regulator on baseboard with VLCD as enable.

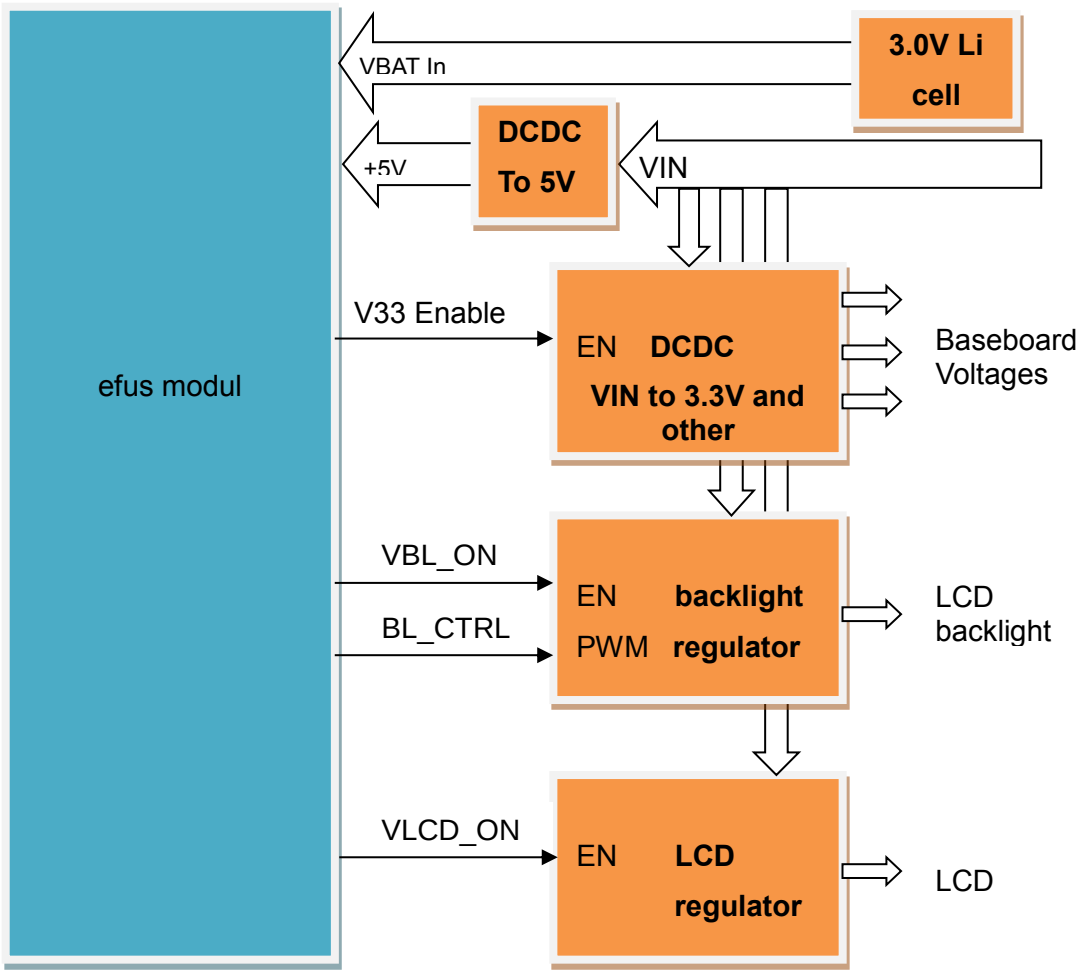

Figure 10: power tree

7 Connect RGB LCD

Connecting a 18bit RGB Display is easy R0 to R0, … B5 to B5.
Please check the datasheet for connecting DE or HSYNC/VSYNC. Some displays with both signals are supporting just DE mode **or** HSYNC/ VSYNC mode. Connecting both is causing the display to malfunction.

Connecting a display with more color lines needs to connect the MSBs together and sharing the LSBs. That means like the following table for color red for a 24bit display:

display signal	**efus signal**
R7 (MSB)	R5 (MSB)
R6	R4
R5	R3
R4	R2
R3	R1
R2	
R1	R0 (LSB)
R0 (LSB)	

Some efus modules supporting 24 color bits with special software and on a not-standard pinout. Minimum quantity required. Please contact sales@fs-net.de for details.

8 EMI/ ESD

On our reference schematic is many ESD and EMI protection included.

Depends your system shielding, external connectors and cables it could be necessary to add metal shields and shielded cables.

Especially a RGB display does produce a lot of EMI emission. Please add serial resistor or ferrite in all signals lines and place them near to the MXM connector. Adjust values depend the signal requirements on the display and EMI results. Route all traces impedance controlled and avoid stubs (every stub will work as antenna).

Using a shielded cable to the display will also reduce EMI.

All signals with outer case connectors should also have an EMI and ESD protection.

There are helpful guides like

Murata's "EMI Supression Filter Application Guide"

and NXP's "Application guide: ESD protection"

We always recommend a metal case with a separated shield ground. Shield ground shouldn't direct connect with signal ground; the best way is to have multiple points to add capacitors, resistors and ferrite beads to make a connection between shield and signal ground.

The right values have to be find on the ESD and EMV certification measurement.

All connector cases should be connect together with the metal case and connect with a single earth wire to the earth ground.

Especially using the LCD RGB signals is critical for EMI. We recommend a strictly impedance controlled PCB, using signal filters like Murata NFA31GD4704704D and a short cable to the panel.

9 Cooling

Depends your efus board power consumption on your application, your airflow and your air temperature several cooling actions could be necessary. In some cases a heat sink on CPU could be enough. Otherwise it needs active airflow or heat pipe solution or a heat spreader to the case with graphite paper.

For a calculation please refer the datasheet of the efus module.

A good description to calculate a heat sink can be found on the Fischerelektronik catalog f.cool on the pages A2 ff.

10 Appendix

List of Figures

Important Notice

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