LVDS Adapter

NetDCU-ADP/LVDS1

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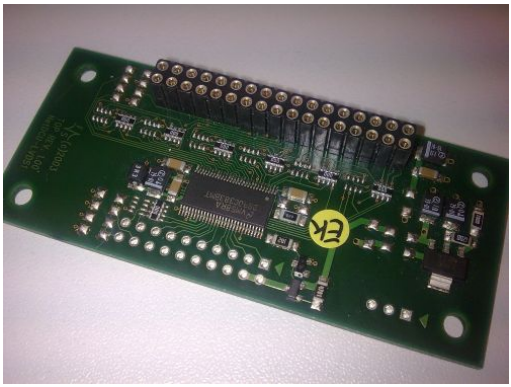
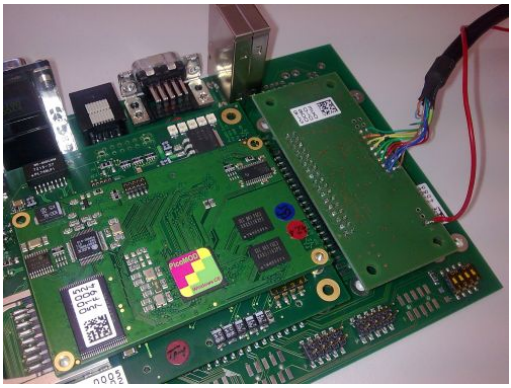
1 Overview

The LVDS adapter NetDCU-ADP/LVDS1 provides an interface to a LC display with LVDS inputs. Displays with a supply voltage of 3.3V or 5V can be connected
The color depth is preconfigured to 6 Bit (8 bit is LVDS2).





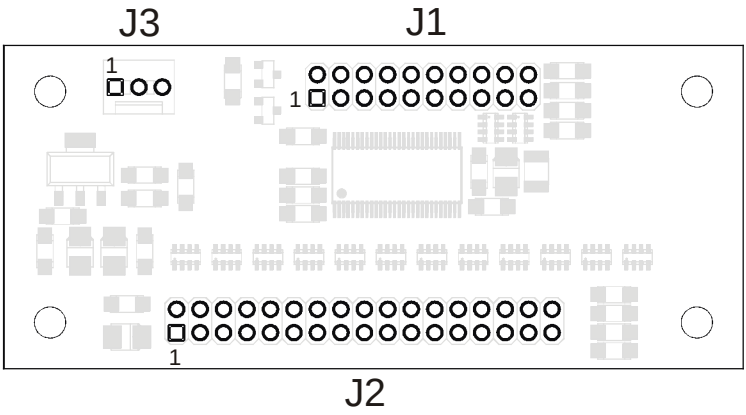
Supported display configurations

The LVDS adapter supports most common configurations for 6 and 8 bit color depth.
The input supports 6 bit digital RGB. The output is preconfigured to 6 or 8 bit and is not user changeable.
For proper function the input of the display must use one of the following mappings.

Supported Display Configurations				
			Display Color Depth	
Transmitter Input	LVDS Output	Bit	6 bit	8 bit
TA0	0	0	R0	R0
TA1		1	R1	R1
TA2		2	R2	R2
TA3		3	R3	R3
TA4		4	R4	R4
TA5		5	R5	R5
TA6		6	G0	G0
TB0	1	0	G1	G1
TB1		1	G2	G2
TB2		2	G3	G3
TB3		3	G4	G4
TB4		4	G5	G5
TB5		5	B0	B0
TB6		6	B1	B1
TC0	2	0	B2	B2

Supported Display Configurations				
			Display Color Depth	
Transmitter Input	LVDS Output	Bit	6 bit	8 bit
TC1		1	B3	B3
TC2		2	B4	B4
TC3		3	B5	B5
TC4		4	Hsync/High	Hsync/High
TC5		5	Vsync/High	Vsync/High
TC6		6	DE	DE
TD0		0		R6
TD1		1		R7
TD2		2		G6
TD3	3	3	Not Used	G7
TD4		4		B6
TD5		5		B7
TD6		6		

Figure 0.1: Top view

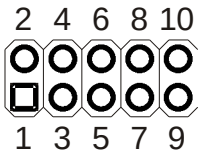


2 Connections

2.1 Connectors

All connections prepared for two-row connectors on the NetDCU5 are treated as follow.
Pin 1 is marked by a square pad.
The row with pin 1 contains all odd-numbered pins (1, 3, 5, 7, etc.), and, corresponding to this, the row without pin 1 contains all even-numbered pins (2, 4, 6, 8, etc.).

Figure 2.1: Example for counting on connectors



2.2 J2 NetDCU Interface

J2 NetDCU Interface		
Pin	**Signal**	**Function**
1	GND	Signal Ground
2	R1	Red Bit 1
3	R0	Red Bit 0 (LSB)
4	G5	Green Bit 5 (MSB)
5	G4	Green Bit 4
6	G3	Green Bit 3
7	G2	Green Bit 2
8	GND	Signal Ground
9	B3	Blue Bit 3
10	B2	Blue Bit 2
11	B1	Blue Bit 1
12	B0	Blue Bit 0 (LSB)
13	G1	Green Bit 1
14	G0	Green Bit 0 (LSB)
15	B5	Blue Bit 5 (MSB)
16	B4	Blue Bit 4
17	GND	Signal Ground
18	---	
19	CLP	Pixel Clock
20	FRP	Frame Impulse, Vsync
21	M	Display Enable Signal

J2 NetDCU Interface		
Pin	**Signal**	**Function**
22	LIP	Line Impulse, Hsync
23	DEN	Display ON
24	GND	Signal Ground
25	VCC	Power Supply +3.3V (*)
26	---	
27	---	
28	GND	Signal Ground
29	---	
30	---	
31	R2	Red Bit 2
32	R3	Red Bit 3
33	R4	Red Bit 4
34	R5	Red Bit 5 (MSB)

(*) Warning: the LCD power supply on the NetDCU must be switched to 3.3V. A higher voltage can destroy the device

2.3 J1 LVDS Interface

J1 LVDS Interface		
Pin	**Signal**	**Function**
1	Tx0-	Negative LVDS Output 0
2	V_{LCD}	Power Supply LCD
3	Tx0+	Positive LVDS output 0
4	V_{LCD}	Voltage supply LCD
5	Tx1-	Negative LVDS output 1
6	GND	Signal Ground
7	Tx1+	Positive LVDS output 1
8	GND	Signal Ground
9	Tx2-	Negative LVDS output 2
10	GND	Signal Ground
11	Tx2+	Positive LVDS output 2
12	GND	Signal Ground
13	TxCLK-	Negative LVDS clock
14	GND	Signal Ground
15	TxCLK+	Positive LVDS clock
16	GND	Signal Ground
17	Tx3-/GND(*)	Negative LVDS output 3 /Ground
18	S1	Configuration output 1
19	Tx3+/GND(*)	Positive LVDS output 3 / Ground
20	S2	Configuration output 2

(*) 8 bit: Tx3, 6bit: GND

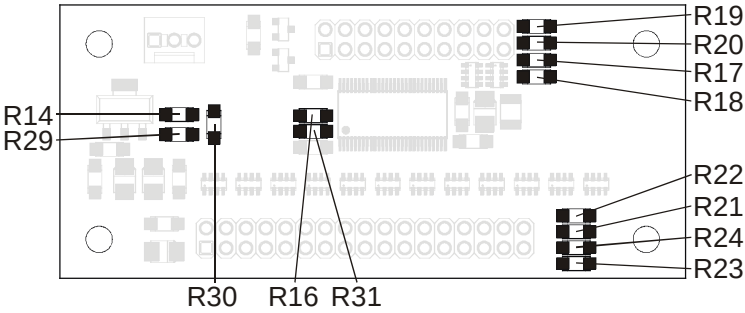
2.4 J3 Power Supply

J3 Power Supply	
Pin	**Function**
1	+5V ±5% DC
2	---
3	Power Ground

3 Configuration LVDS Adapter

The LVDS adapter can be configured for the use with different LC displays.

Figure 3.1: Top view



3.1 Power-Supply

The NetDCU LCD-Power-Supply **must** be set to **3.3V**, a higher voltage can destroy the device.

Display-Power-Supply	R14	R29	R30
3.3V	X		X
5V	X	X	

3.2 Display Color Depth

The color depth is preconfigured an can not be changed

3.3 Hsync/Vsync

Hsync and Vsync signals can be connected to transmitter with jumpers R21 and R23. If these signals are not used by the display, the transmitter inputs can be tied to high level with jumpers R22 and R24.

Configuration	R21	R22	R23	R24
Hsync/Vsync used	X		X	
Hsync/Vsync not used		X		X

Rxx Jumper, 0Ω Resistor Type 1206

3.4 Display Configuration Outputs S1, S2

The outputs S1 and S2 can each be tied to the display supply voltage V_{LCD}, to ground, or can be left open for display-specific configurations.

Configuration	R17	R18
S1 on V_{LCD}	X	
S1 on GND		X
S1 open		

Configuration	R19	R20
S2 on V_{LCD}	X	
S2 on GND		X
S2 open		

Rxx Jumper, 0Ω Resistor Type 1206

Warning! You must not use both Resistors for one output! The device can be damaged!

3.5 Strobe Edge

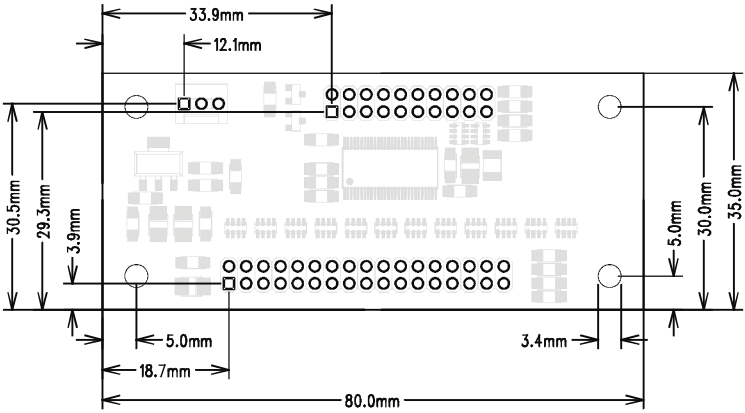
The LVDS adapter can be configured for the rising or falling edge of the pixel clock

Configuration	R16	R31
Rising edge		X
Falling edge	X	

Rxx Jumper, 0Ω Resistor Type 1206

4 Dimensions

Figure 4.1: Top view



All values can have tolerances of ±0.5mm.

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