Hardware Documentation

efusMX93

for HW Revision 1.00

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Elektronik Systeme

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About This Document

This document describes how to use the efusMX93 (further named as module) with mechanical and electrical information. The latest version of this document can be found at: www.fsembedded.com.

ESD Requirements

All F&S hardware products are electrostatic discharge (ESD) sensitive. All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD sensitive material in ESD unsafe environments. Negligent handling will harm the product and warranty claims become void.

Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

History

Version	Date	Platform	Added (A) Removed (R) Modified (M)	Chapter	Description	Author
001/08.2025	05.08.2025	-	-	All	Initial Version	SM

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1 Overview

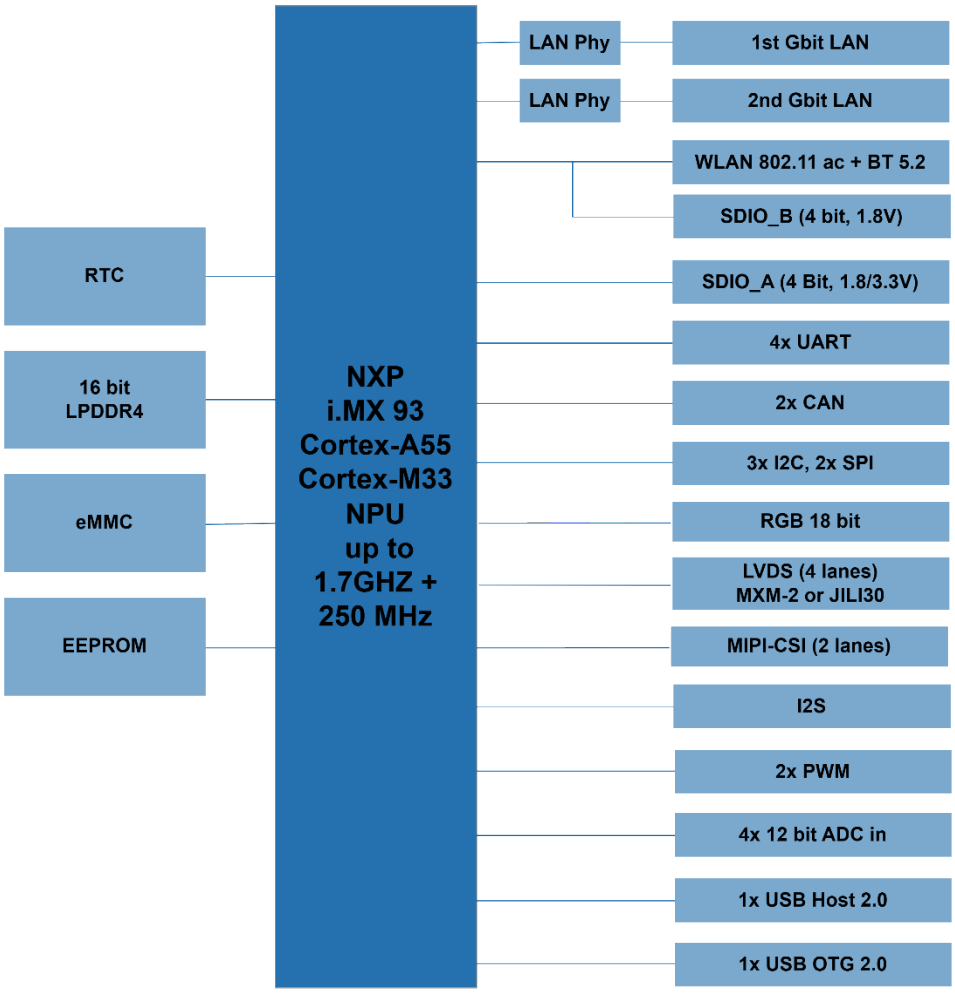
1.1 General Parameter

Parameter	Description
Dimension	62.1 mm x 47.0 mm x 3.6 mm
Weight	≈ 15 g
Operating Temperature	-40.0 °C … +85.0 °C
Mounting Holes	2x Ø 2.6 mm

Table 1: General parameter

1.2 Block Diagram

The following figure shows the intended functionalities of the module.



Note: The availability depends on the configuration.

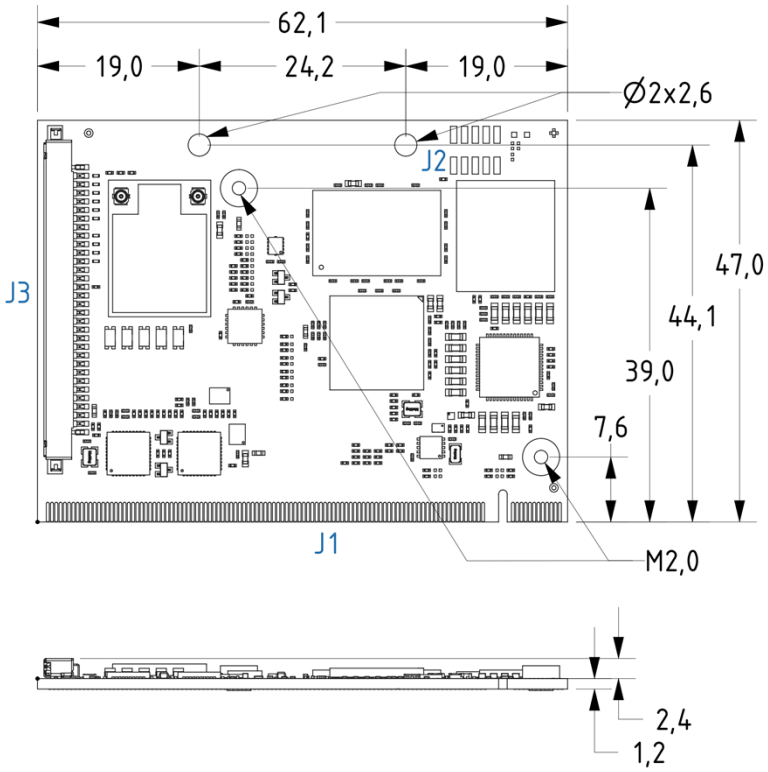
Figure 1: Block diagramm

Additionally, F&S supports customized solutions with a different IOMUX.

Note: This may lead to completely different configurations. Please contact sales@fs-net.de for further information.

1.3 Dimensions and Connectors

1.3.1 Technical Drawing



Note: All dimensions are in mm.

Figure 2: Technical drawing

1.3.2 Connectors

Ref.	Description	Connector Type	Counter Part
J1	Edge Connector	MXM-2, 0.5 mm Pitch, 230 pins	Foxconn, AS0B326-S78N-7F[1]
J2	JTAG	2x5 pos RM: 1.27 mm	
J3	Display	Hirose, MDF76GW-30S-1H	JAE, FI-X30H[1]

[1]Connectors and preassembled cables are available for purchase at www.fsembedded.com.

Table 2: Connector description

1.4 Power and Management

1.4.1 Power Supply

The following table shows the intended use of the power pins on the module.

Contact #	Contact Name	I/O	Voltage	Comments
1, 2, 3, 4, 5, 6	VCC_IN_5V	P	5.0 V	Main power supply input
9	V_BAT	P	3.0 V	RTC supply input[1,2]
10	V33_OUT_IO	PO	3.3 V	Intended to supply carrier peripherals max. current: 500 mA
26	SD_A_VCC	PO	1.8 V 3.3 V	SDIO_A I/O reference voltage (switchable) max. current: 100 mA
71	SD_B_VCC	PO	1.8 V	SDIO_B I/O reference voltage max. current: 100 mA
134	DVI_DDC_VOUT	PO	3.3 V	Display supply output max. current: 100 mA
198	ETH_VLED_OUT	PO	3.3 V	Intended to supply ETH LINK LED(s) max. current: 50 mA
7, 8, 27, 30, 33, 39, 45, 46, 51, 57, 63, 64, 75, 80, 85, 90, 91, 95, 100, 101, 110, 114, 115, 118, 122, 128, 129, 136, 143, 147, 159, 160, 172, 181, 184, 185, 199, 209, 210, 215, 218, 224, 229, 230	GND			

Table 3: PWR (pin description)

[1] RTC_PWR may be sourced from a Carrier based Li-cell or Super Cap.

[2] Polarity and overcurrent protection on module.

1.4.2 System Control

The following table shows the intended use of the control pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
13	I0OUT_ADC_IN	ONOFF	O	1.8 V	PU 100k, behavior depends on the configuration. A button to GND can be directly connected[1].
12	RESET_IN#	PMIC_RST_B	I	1.8 V	PU 100k, logic LOW resets the module
14	RESET_OUT#	I2C IO Exp.: P0_5	O	3.3 V	
48	EXT_PROG	BOOT_MODE[0]	I	3.3 V	PU 10k HIGH/FLOAT: module boots from internal fuses LOW: module is in USB Serial Download mode
36	RESERVED	TAMPER0	I	1.8 V	

Table 4: System Control (pin description)

[1] Debounced inside of the CPU.

1.5 Interfaces

1.5.1 JTAG (J2)

JTAG is for debug only. The following table shows the intended use of the JTAG[1,2] pins on the module, on connector J2.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
1	V_1V8		P	1.8 V	
2	JTAG_TMS(SWDIO)	DAP_TMS_SWDIO	I	1.8 V	firmly connected to UART_B_RTS[3]
3	GND				
4	JTAG_TCK(SWCLK)	DAP_TCLK_SWCLK	I	1.8 V	firmly connected to UART_B_CTS[3]
5	GND				
6	JTAG_TDO(SWO)	DAP_TDO_TRACESWO	O	1.8 V	firmly connected to UART_B_TX[3]
8	JTAG_TDI	DAP_TDI	I	1.8 V	firmly connected to UART_B_RX[3]
9	GND				
10	RESET_IN#		I	1.8 V	

Table 5: JTAG (J2 pin description)

[1] Do not put the JTAG of the module in a JTAG chain, because different power sequence and power level could kill the CPU.

[2] In addition to JTAG, one will have access to the Cortex®-A55 and Cortex®-M33 cores via serial console. See chapter UART.

[3] Do not use UART_B together with JTAG at the same time.

1.5.2 UART

The module provides up to four Universal Asynchronous Receiver Transmitter (UART) ports. The following table shows the use of the UART related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
92	UART_A_RX	UART1_RXD[1]	I	3.3 V	Cortex®-A55 debug
94	UART_A_TX	UART1_TXD	O	3.3 V	PD 10k + LOGIC[2], Cortex®-A55 debug dual function: BOOT_MODE[0][1],
102	UART_B_RX[3]	DAP_TDI		3.3 V	firmly connected to JTAG_TDI[4]
104	UART_B_TX[3]	DAP_TDO_TRACESWO		3.3 V	firmly connected to JTAG_TDO(SWO)[4]
106	UART_B_RTS[3]	DAP_TMS_SWDIO		3.3 V	firmly connected to JTAG_TMS(SWDIO)[4]
108	UART_B_CTS[3]	DAP_TCLK_SWCLK		3.3 V	firmly connected to JTAG_TCK(SWCLK)[4]
15	UART_C_RX5	ENET1_RD0		3.3 V	Cortex®-M33 debug
17	UART_C_TX[5]	ENET1_TD0		3.3 V	Cortex®-M33 debug
19	UART_C_RTS[5,6]	ENET1_TD1		3.3 V	
21	UART_C_CTS[5,6]	ENET1_RD2		3.3 V	
96	UART_D_RX	UART2_RXD[1]	I	3.3 V	
98	UART_D_TX	UART2_TXD	O	3.3 V	PD 10k, dual function: BOOT_MODE[1][1]

Table 6: UART (pin description)

[1] The i.MX93 pad is part of the BOOT_CFG. Make sure not to overrule the intended configuration during the startup.

[2] See the information about EXT_PROG in chapter System Control.

[3] Not available when Bluetooth is used.

[4] Do not use UART_B together with JTAG at the same time.

[5] Not available together with Ethernet_B.

[6] Not available when I2S is used.

1.5.3 SDIO

The module provides two Secure Digital Input Output (SDIO) interfaces. The following table shows the use of the SDIO related pins on the module.

Note: For specification and licensing please refer to the website of the SD Association http://www.sdcard.org.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
24	SDIO_A_CMD	SD2_CMD	I/O	1.8 V[1] 3.3 V[1]	
28	SDIO_A_CLK	SD2_CLK	O	1.8 V[1] 3.3 V[1]	
32	SDIO_A_D0	SD2_DATA0	I/O	1.8 V[1] 3.3 V[1]	
34	SDIO_A_D1	SD2_DATA1	I/O	1.8 V[1] 3.3 V[1]	
20	SDIO_A_D2	SD2_DATA2	I/O	1.8 V[1] 3.3 V[1]	
22	SDIO_A_D3	SD2_DATA3	I/O	1.8 V[1] 3.3 V[1]	
18	SDIO_A_CD#	SD2_CD_B	I	1.8 V[1] 3.3 V[1]	PU 10k
16	SDIO_A_WP	SD2_RESET_B	I	1.8 V[1] 3.3 V[1]	
69	SDIO_B_CMD[2]	SD3_CMD	I/O	1.8 V	
73	SDIO_B_CLK[2]	SD3_CLK	O	1.8 V	
77	SDIO_B_D0[2]	SD3_DATA0	I/O	1.8 V	
79	SDIO_B_D1[2]	SD3_DATA1	I/O	1.8 V	
65	SDIO_B_D2[2]	SD3_DATA2	I/O	1.8 V	
67	SDIO_B_D3[2]	SD3_DATA3	I/O	1.8 V	
83	SDIO_B_CD#	I2C IO Exp.: P1_5	I	3.3 V	
81	SDIO_B_WP	I2C IO Exp.: P1_6	I	3.3 V	

Table 7: SDIO (pin description)

[1] As SDIO_A is intended to be used with SD/MMC cards, the I/O voltage is dynamically switchable between 3.3 V & 1.8 V on the module. The level of SDIO_A_IOPWR depends on the internal signal SD2_VSEL (CPU pad: SD2_VSELECT):

- SD2_VSEL = LOW: SDIO_A_IOPWR = 3.3 V (default)
- SD2_VSEL = HIGH: SDIO_A_IOPWR = 1.8 V

[2] Not available when the Wi-Fi Module is mounted.

1.5.4 PWM

The module provides two free programmable Pulse Width Modulation (PWM) signals[1,2]. The following table shows the use of the PWM related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
25	PWM_A	GPIO_IO24	O	3.3 V	
87	VBL_PWM	GPIO_IO26	O	3.3 V	

Table 8: PWM (pin description)

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the PWM contacts it must be ensured that no voltage is applied on any PWM pin on a non-powered module.

1.5.5 Analog Signals

The module provides four 12-bit Analog to Digital Converter (ADC). The following table shows the use of the ADC related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
38	RESERVED2	ADC_IN0	I	0 … 1.8 V	
40	RESERVED3	ADC_IN1	I	0 … 1.8 V	
42	RESERVED4	ADC_IN2	I	0 … 1.8 V	
44	RESERVED5	ADC_IN3	I	0 … 1.8 V	

Table 9: ADC (pin description)

1.5.6 SPI

The module provides two Serial Peripheral Interface (SPI) ports. The following table shows the use of the SPI related pins on the module.

Because of no more available SPI Interfaces on the CPU, the second SPI (SPI_B) is firmly connected to SPI_A. It is intended to supply existing products with an SPI interface on the SPI_B contacts.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
68	SPI_A_MOSI	SAI1_TXC	I/O	3.3 V	
66	SPI_A_MISO	SAI1_RXD0	I/O	3.3 V	
70	SPI_A_SCLK	SAI1_TXD0[1]	I/O	3.3 V	PD 10k, dual function: BOOT_MODE[3][1]
72	SPI_A_CS1#	SAI1_TXFS[1]	I/O	3.3 V	PD 10k, dual function: BOOT_MODE[2][1]
74	SPI_A_CS2#	I2C IO Exp.: P1_7	O	3.3 V	
76	SPI_A_IRQ1#	PDM_BIT_STREAM1	O	3.3 V	
78	SPI_A_IRQ2#	GPIO_IO28	O	3.3 V	
52	SPI_B_MOSI	SAI1_TXC	I	3.3 V	firmly connected to SPI_A_MOSI
50	SPI_B_MISO	SAI1_RXD0	O	3.3 V	firmly connected to SPI_A_MISO
54	SPI_B_SCLK	SAI1_TXD0[1]	I/O	3.3 V	firmly connected to SPI_A_SCLK PD 10k, dual function: BOOT_MODE[3][1]
56	SPI_B_CS1#	ENET1_RXC[2]	O	3.3 V	
30	SPI_B_IRQ1#	ENET1_RD1[2]	O	3.3 V	

Table 10: SPI (pin description)

[1] The i.MX93 pad is part of the BOOT_CFG. Make sure not to overrule the intended configuration during the startup.

[2] Not available together with Ethernet_B.

1.5.7 I2S

The module provides one Inter-IC Sound (I2S) interface[1, 2]. The following table shows the use of the I2S related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
112	I2S_MCLK	ENET1_RD2	O	3.3 V	
116	I2S_LRCLK	ENET1_TX_CTL	I/O	3.3 V	
120	I2S_SCLK	ENET1_TXC	I/O	3.3 V	
124	I2S_TXD	ENET1_RX_CTL	O	3.3 V	
126	I2S_RXD	ENET1_TD3	I	3.3 V	

Table 11: I2S (pin description)

[1] Not available together with Ethernet_B.

[2] Not available when UART_C with flow control is used.

1.5.8 CAN FD

The module provides two Controller Area Network Interfaces with Flexible Data-Rate (CAN FD). The following table shows the use of the CAN related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
29	CAN_A_TX	PDM_CLK	O	3.3 V	
31	CAN_A_RX	PDM_BIT_STREAM0	I	3.3 V	
35	CAN_B_TX[1]	GPIO2_IO25	O	3.3 V	
37	CAN_B_RX[1]	GPIO2_IO27	I	3.3 V	

Table 12: CAN FD (pin description)

1.5.9 USB

The module provides two Universal Serial Busses (USB), including controllers and PHYs. The following table shows the use of the USB related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
214	USB_A_D_N	USB2_D_N	I/O	USB	
216	USB_A_D_P	USB2_D_P	I/O	USB	
212	USB_A_PWR	I2C IO Exp.: P0_2	O	3.3 V	USB (Host) power enable
225	USB_DEV_D_N	USB1_D_N	I/O	USB	
227	USB_DEV_D_P	USB1_D_P	I/O	USB	
223	USB_DEV_ID	USB1_ID	I	1.8 V	
217	USB_DEV_VBUS	USB1_VBUS	I	3.3 V	USB VBUS detection on the PHY port 1[1]
219	USB_DEV_PWR	I2C IO Exp.: P0_3	O	3.3 V	USB (OTG) power enable

Table 13: USB (pin description)

[1] Must always be connected to the respective USB VBUS rail.

1.5.10 I2C

The module provides three Inter-Integrated Circuit (I2C) interfaces which are connected to the following components.

I2C	Connected To	Address	Comments
A	I2C_A		general I2C on carrier
	EEPROM	0x50	EEPROM on the module (accessible from carrier)
B	I2C_B		general I2C on carrier
	Display		Connected to J3
C	I2C_C		general I2C on carrier
	GPIO Expander[1]	0x20	GPIO Expander on the module
	RTC	0x51	Real Time Clock on the module
	Display		Optional connected to J3
	PMIC	0x25	Power Management IC on the module

Table 14: I2C (usage)

[1] Used GPIO expander type: NXP, PCAL6416A

The following table shows the use of the I2C related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
155	I2C_A_SCL	I2C1_SCL	I/O	3.3 V	PU 2k49
151	I2C_A_SDA	I2C1_SDA	I/O	3.3 V	PU 2k49
153	I2C_A_IRQ#	GPIO_IO29	I/O	3.3 V	
157	I2C_A_RST#	I2C IO Exp.: P1_3	I/O	3.3 V	
84	I2C_B_SCL	GPIO_IO22	I/O	3.3 V	PU 2k49

82	I2C_B_SDA	GPIO_IO23	I/O	3.3 V	PU 2k49
86	I2C_B_IRQ#	CCM_CLKO3[1]	I/O	3.3 V	
88	I2C_B_RST#	I2C IO Exp.: P1_4	I/O	3.3 V	
132	I2C_C_SCL	I2C2_SCL	I/O	3.3 V	PU 2k49
130	I2C_C_SDA	I2C2_SDA	I/O	3.3 V	PU 2k49

Table 15: I2C (pin description)

[1] Not available when the Wi-Fi Module is mounted

1.5.11 MIPI CSI

The module provides one 2 lane Camera Serial Interface (CSI), defined by the Mobile Industry Processor Interface Alliance (MIPI):

- complaint with MIPI CSI-2 specification v1.3 and MIPI D-PHY specification v1.2.

The following table shows the use of the MIPI CSI related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
C1	CSI_A_DATA0_N	MIPI_CSI1_D0_N	I	MIPI CSI	
B1	CSI_A_DATA0_P	MIPI_CSI1_D0_P	I	MIPI CSI	
A2	CSI_A_DATA1_N	MIPI_CSI1_D1_N	I	MIPI CSI	
A3	CSI_A_DATA1_P	MIPI_CSI1_D1_P	I	MIPI CSI	
B3	CSI_A_CLOCK_N	MIPI_CSI1_CLOCK_N	I	MIPI CSI	
B4	CSI_A_CLOCK_P	MIPI_CSI1_CLOCK_P	I	MIPI CSI	

Table 16: CSI (pin description)

1.5.12 Display (LVDS) (J1 / J3)

The module provides a single channel (4 lane) Low Voltage Differential Signal (LVDS) interface optional on two connectors.[1]

The following tables show the use of the DISP LVDS related pins on the two connectors.

[1] Option 1: MXM connector J1, option 2: display connector J3

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
148	LVDS_D0_N	LVDS_D0_N	O	LVDS	
146	LVDS_D0_P	LVDS_D0_P	O	LVDS	
144	LVDS_D1_N	LVDS_D1_N	O	LVDS	
142	LVDS_D1_P	LVDS_D1_P	O	LVDS	
140	LVDS_D2_N	LVDS_D2_N	O	LVDS	
138	LVDS_D2_P	LVDS_D2_P	O	LVDS	
156	LVDS_D3_N	LVDS_D3_N	O	LVDS	
154	LVDS_D3_P	LVDS_D3_P	O	LVDS	
152	LVDS_CLK_N	LVDS_CLK_N	O	LVDS	
150	LVDS_CLK_P	LVDS_CLK_P	O	LVDS	

Table 17: DISP LVDS (J1 pin description)

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
1	LVDS_D0_N	LVDS_D0_N	O	LVDS	
2	LVDS_D0_P	LVDS_D0_P	O	LVDS	
3	LVDS_D1_N	LVDS_D1_N	O	LVDS	
4	LVDS_D1_P	LVDS_D1_P	O	LVDS	
5	LVDS_D2_N	LVDS_D2_N	O	LVDS	
6	LVDS_D2_P	LVDS_D2_P	O	LVDS	
7	GND				

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
8	LVDS_D3_N	LVDS_D3_N	O	LVDS	
9	LVDS_D3_P	LVDS_D3_P	O	LVDS	
10	LVDS_CLK_N	LVDS_CLK_N	O	LVDS	
11	LVDS_CLK_P	LVDS_CLK_P	O	LVDS	
14			GND		
17			GND		
24			GND		
25	I2C_B_SDA	GPIO_IO23	I/O	3.3 V	Optional: I2C_C_SDA
26	DISP_IRQ#	ENET2_MDIO	I	3.3 V	Interrupt input
27	I2C_B_SCL	GPIO_IO22	O	3.3 V	Optional: I2C_C_SCL
28	DISP_RST	I2C IO Exp.: P1_2	O	3.3 V	Reset output
29	V_DISP		PO	3.3 V	Display supply output
30					

Table 18: DISP LVDS (J3 pin description)

1.5.13 Display (RGB)

The module provides a 18-bit Red Green Blue (RGB) interface.

The following tables show the use of the DISP RGB related pins.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
103	LCD_R0	GPIO_IO16	O	3.3 V	
105	LCD_R1	GPIO_IO17	O	3.3 V	
107	LCD_R2	GPIO_IO18	O	3.3 V	
109	LCD_R3	GPIO_IO19	O	3.3 V	
111	LCD_R4	GPIO_IO20	O	3.3 V	
113	LCD_R5	GPIO_IO21	O	3.3 V	
117	LCD_G0	GPIO_IO10	O	3.3 V	
119	LCD_G1	GPIO_IO11	O	3.3 V	
121	LCD_G2	GPIO_IO12	O	3.3 V	
123	LCD_G3	GPIO_IO13	O	3.3 V	
125	LCD_G4	GPIO_IO14	O	3.3 V	
127	LCD_G5	GPIO_IO15	O	3.3 V	
131	LCD_B0	GPIO_IO04	O	3.3 V	
133	LCD_B1	GPIO_IO05	O	3.3 V	
35	LCD_B2	GPIO_IO06	O	3.3 V	
137	LCD_B3	GPIO_IO07	O	3.3 V	
139	LCD_B4	GPIO_IO08	O	3.3 V	
141	LCD_B5	GPIO_IO09	O	3.3 V	
93	LCD_CLK	GPIO_IO00	O	3.3 V	
97	LCD_HSYNC	GPIO_IO03	O	3.3 V	
99	LCD_VSYNC	GPIO_IO02	O	3.3 V	
145	LCD_DE	GPIO_IO01	O	3.3 V	

Table 19: DISP RGB (pin description)

1.5.14 Display (Contrtol)

To control connected displays, the module provides several signals.

The following tables show the use of the DISP control related pins.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
149	VLCD_ON	I2C IO Exp.: P1_0	O	3.3 V	Display enable
89	VBL_ON	I2C IO Exp.: P1_1	O	3.3 V	Backlight enable
87	BL_PWM	GPIO_IO26	O	3.3 V	Backlight brightness control

Table 20: DISP Control (pin description)

1.5.15 Ethernet

The module provides two Media Dependend Interfaces (MDI) ports for 1000Base-T Ethernet[1].

The following tables show the use of the ETH related pins.

[1] Used physical layer chip: Realtek, RTL8211FDI

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
206	ETH_A_D1_N	PHY A: MDIN0	I/O	3.3 V	
208	ETH_A_D1_P	PHY A: MDIP0	I/O	3.3 V	
200	ETH_A_D2_N	PHY A: MDIN1	I/O	3.3 V	
202	ETH_A_D2_P	PHY A: MDIP1	I/O	3.3 V	
194	ETH_A_D3_N	PHY A: MDIN2	I/O	3.3 V	
196	ETH_A_D3_P	PHY A: MDIP2	I/O	3.3 V	
188	ETH_A_D4_N	PHY A: MDIN3	I/O	3.3 V	
190	ETH_A_D4_P	PHY A: MDIP3	I/O	3.3 V	
192	ETH_A_LED_ACT	PHY A: LED1	O	3.3 V	
204	ETH_A_LED_LINK	PHY A: LED2	O	3.3 V	
180	ETH_B_D1_N[2]	PHY B: MDIN0	I/O	3.3 V	
182	ETH_B_D1_P[2]	PHY B: MDIP0	I/O	3.3 V	
174	ETH_B_D2_N[2]	PHY B: MDIN1	I/O	3.3 V	
176	ETH_B_D2_P[2]	PHY B: MDIP1	I/O	3.3 V	
168	ETH_B_D3_N[2]	PHY B: MDIN2	I/O	3.3 V	
170	ETH_B_D3_P[2]	PHY B: MDIP2	I/O	3.3 V	
162	ETH_B_D4_N[2]	PHY B: MDIN3	I/O	3.3 V	
164	ETH_B_D4_P[2]	PHY B: MDIP3	I/O	3.3 V	
166	ETH_B_LED_ACT[2]	PHY B: LED1	O	3.3 V	
178	ETH_B_LED_LINK[2]	PHY B: LED2	O	3.3 V	

Table 21: ETH (pin description)

[2] Not available when I2S and/or UART C is used.

1.6 Internal Peripherals on the Module

1.6.1 LPDDR4

The module contains one 16-bit LPDDR4 SDRAM which operates with up to 3733 MT/s.

1.6.2 eMMC

The module contains one Embedded MultiMedia Card (eMMC) Flash memory. eMMCs have limited erasing cycles, and the data retention depends on the temperature. It is important to know that high temperatures above 50°C significantly impact the data retention of the eMMC[1], independently whether the device is powered or not.

[1] Please contact us for more information about data retention on eMMCs in high temperature environments.

1.6.3 RTC

The module contains a Real Time Clock (RTC, Type: PCF85263ATL)[1] which is connected to the internal I2C bus (I2C_INT, address: 0x51). The time can be maintained by applying a suitable voltage to V_RTC even if the module itself is not powered.

[1] Cause the accuracy is limited by the crystal, the RTC could drift some seconds per day.

1.6.4 EEPROM

The module contains a 64Kb Electrically Erasable Programmable Read-Only Memory (EEPROM) (Type: N24S64B) which is connected to I2C_A (address: 0x50).

2 Characteristics

2.1 Absolute Maximum Ratings[1]

Parameter	Description	Min	Max	Unit
V_{5V}	main power input voltage at the V_5V_IN pins	-0.50	6.00	V
V_{RTC}	RTC battery input voltage at the RTC_PWR pin	-0.50	6.50	V
V_{IO}	general I/O voltage (V_{DD} … nominal I/O voltage)	-0.30	V_{DD} + 0.30	V
USB VBUS	PHY detection signal of USB port supply voltage on the carrier	-0.30	5.50	V

Table 22: Absolute Maximum Ratings

[1] Stresses beyond the listed values may affect reliability or cause permanent damage to the module.

2.2 Recommended Operating Conditions

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{5V}	main power input[1]		4.50	5.00	5.50	V
I_{5V}					2.70	A
V_{RTC}	RTC battery input	contact: **J1.9** V_{RTC} = 3.0 V	1.20	3.00	5.50	V
I_{RTC}				350	480	nA
USB VBUS	PHY detection of USB VBUS	contact: **J1.217**		5.00		V
$V_{33\_OUT\_IO}$	supply output (for carrier peripherals)	contact: **J1.10**		3.30		V
$I_{V33\_OUT\_IO}$					500	mA
$V_{V\_ETH\_3V3}$	supply output (ETH I/O reference)	contact: **J1.198**		3.30		V
$I_{V\_ETH\_3V3}$					100	mA
$V_{DVI\_DDC\_VOUT}$	supply output (DISP I/O reference)	contact: **J1.134**		3.30		V
$I_{VDVI\_DDC\_VOUT}$					100	mA
$V_{SD\_A\_VCC}$	supply output (SDIO_A I/O reference)	contact: **J1.26**		1.80	3.30	V
$I_{VSD\_A\_VCC}$					100	mA
$V_{SD\_B\_VCC}$	supply output (SDIO_B I/O & ADC reference)	contact: **J1.71**		1.80	3.30	V
$I_{VSD\_B\_VCC}$					100	mA
V_{IH}	I/O high-level input voltage	V_{DD} = 1.8 V / 3.3 V	0.7 · V_{DD}	V_{DD}	V_{DD} + 0.2	V
V_{IL}	I/O low-level I/O input voltage		-0.20		0.3 · V_{DD}	V
V_{OH}	I/O high-level output voltage		0.8 · V_{DD}		V_{DD}	V
V_{OL}	I/O low-level I/O output voltage		0		0.2 · V_{DD}	V
I_{GPIO_OUT}	I/O drive strength (general)				8	mA
V_{ADC_IN}	ADC input voltage range		0		1.80	V
$T_{OPERATE}$	operating temperature range[2]	C TEMP grade	0		70	°C
		I TEMP grade	-25		85	°C
		XI TEMP grade	-40		85	°C
$T_{STORAGE}$	storage temperature range		-40		85	°C
$t_{STORAGE}$	storage time	no environmental control		6	months	
		T_{AMB} = 25 °C ± 5 °C humidity max. 60 %		12	months	

Table 23: Recommended Operating Conditions

[1] The module is tested and validated within the specified range.

[2] An external cooling solution may be required to cover the entire range.

3 Packaging & Labels

3.1 ESD

All F&S electrostatic discharge sensitive (ESDS) products are marked and will be shipped in ESD protective packaging.

3.2 Serial Number

All shipped F&S products are labeled with a matrix code sticker that includes the serial number. For product information visit www.fsembedded.com/en/support/serial-number-info-and-rma/.

4 Appendix

4.1 Second source rules

The qualifications of products from a second source are done autonomously by F&S. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible. F&S does not use broker components without the consent of the customer.

4.2 RoHS and REACH statement

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