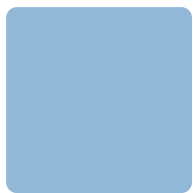


Hardware Documentation

ADP-OSMBB2 *for HW Revision 1.00*

Version 001/08.2025

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About This Document

This document describes how to use the ADP-OSMBB2 with mechanical and electrical information. The latest version of this document can be found at: www.fseembedded.com.

ESD Requirements



All F&S hardware products are electrostatic discharge (ESD) sensitive. All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD sensitive material in ESD unsafe environments. Negligent handling will harm the product and warranty claims become void.

Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

History

Version	Date	Platform	Added (A) Removed (R) Modified (M)	Chapter	Description	Author
001/08.2025	31.07.20250 5.08.2025	-	-	All	Initial Version	TM

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1 Overview

1.1 Additional Documentation

The latest versions of the documents can be found on www.fseembedded.com.

1.2 Compatible OSM Modules

The following F&S OSM modules are compatible with this adapter:

- FS 8ULP OSM-SF

1.3 General Parameter

Parameter	Description
Dimension	35.0 mm x 40.0 mm x 4.6 mm
Weight	≈ 50.0 g
Operating Temperature	-25.0 °C ... +85.0 °C also depends on OSM
Mounting Holes	2x Ø 2.3 mm

Table 1: General parameter

1.4 Dimensions and Connectors

1.4.1 Technical Drawing

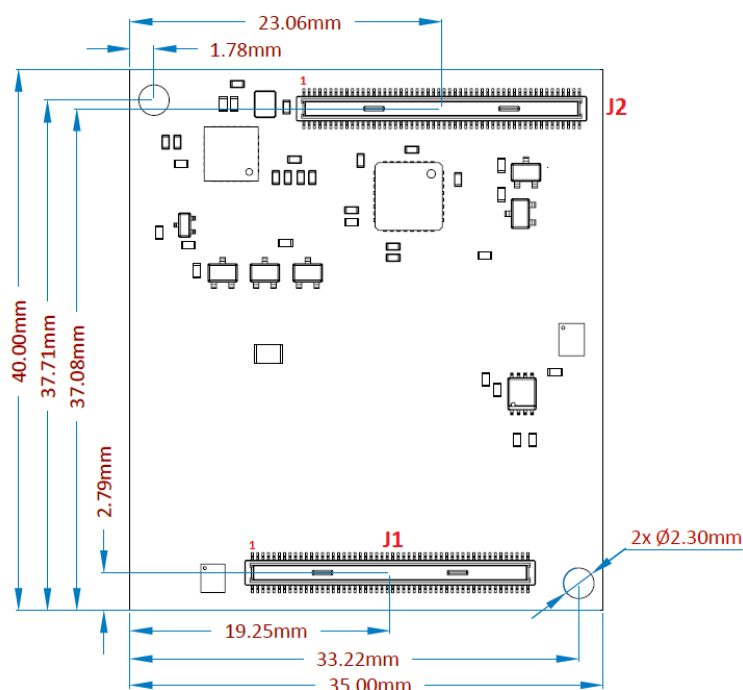


Figure 1: Technical drawing

1.4.2 Connectors

Ref.	Description	Connector Type	Counter Part
J1	Board to board connector	DF40C-100DP-0.4V(51)	DF40C-100DS-0.4V(51)
J2	Board to board connector	DF40C-100DP-0.4V(51)	DF40C-100DS-0.4V(51)

¹Connectors and preassembled cables are available for purchase at www.fseembedded.com.

Table 2: Connector description

2 Connector Signal Description

2.1 Contact type definition

Contact Type	Description
I	Input to the module
O	Output from the module
I/O	Bi-directional input / output signal
N.C.	Not connected
PU	Pull up resistor
PD	Pull down resistor

Table 3: Contact Types

2.2 Connector J1

Pin	Signal	OSM PIN	Voltage	I/O	PU/PD	Description
1	I2C_CAM_IRQ	D17	3.3V	I		I ² C interrupt
2	GPIO_B_5	J19	1.8V	O		
3	I2C_CAM_CLK	C4	3.3V	I/O		I ² C Clock
4	I2C_A_SCL	AA15	1.8V	I/O		I ² C channel A Clock
5	I2C_CAM_SDA	C3	3.3V	I/O		I ² C Data
6	I2C_A_SDA	AA16	1.8V	I/O		I ² C channel A Data
7	GPIO_B_6	K19	1.8V	I/O		
8	GND					
9	GPIO_C_5	F4	1.8V	I/O		Display backlight enable
10	CAN_A_RX	AB17	3.3V	O		CAN channel A receive
11	PWM_0	E18	1.8V / 3.3V	O		Display backlight pwm
12	CAN_A_TX	AC17	3.3V	I		CAN channel A Transmit
13	GPIO_C_4	F3	1.8V / 3.3V	I/O		Power Enable for display
14	N.C.	-				
15	GND					
16	N.C.	-				
17	DSI_A_CLK_P	AB7	MIPI DSI	O		Display Serial Interface Clock positive
18	UART_A_RXD	D22	3.3V	O		RS232 channel A receive
19	DSI_A_CLK_N	AB8	MIPI DSI	O		Display Serial Interface Clock negative
20	UART_A_TXD	D23	3.3V	I		RS232 channel A transmit
21	GND					
22	UART_B_RTS	D15	3.3V	O		RS232 channel B ready to send
23	DSI_A_DATA0_P	AB10	MIPI DSI	O		Display Serial Interface Data 0 positive

Pin	Signal	OSM PIN	Voltage	I/O	PU/PD	Description
24	UART_B_CTS	C14	3.3V	O		RS232 channel B clear to send
25	DSI_A_DATA0_N	AB11	MIPI DSI	O		Display Serial Interface Data 0 negative
26	UART_B_RXD	D14	3.3V	O		RS232 channel B receive
27	GND					
28	UART_B_TXD	D13	3.3V	I		RS232 channel B transmit
29	DSI_A_DATA1_P	AC8	MIPI DSI	O		Display Serial Interface Data 1 positive
30	N.C.	-				
31	DSI_A_DATA1_N	AC9	MIPI DSI	O		Display Serial Interface Data 1 negative
32	N.C.	-				
33	GND					
34	UART_D_RXD	A22	3.3V	O		RS232 channel D receive
35	DSI_A_DATA2_P	AC5	MIPI DSI	O		Display Serial Interface Data 2 positive
36	UART_D_TXD	B23	3.3V	I		RS232 channel D transmit
37	DSI_A_DATA2_N	AC6	MIPI DSI	O		Display Serial Interface Data 2 negative
38	GND					
39	GND					
40	N.C.	-				
41	DSI_A_DATA3_P	AB4	MIPI DSI	O		Display Serial Interface Data 3 positive
42	N.C.	-				
43	DSI_A_DATA3_N	AB5	MIPI DSI	O		Display Serial Interface Data 3 negative
44	GPIO_B_4	H19	1.8V	I/O		
45	GND					
46	GPIO_B_3	G19	1.8V	I/O		
47	N.C.	-				
48	I2C_D_SCL	AA15	3.3V	I/O		I ² C channel D Clock
49	N.C.	-				
50	I2C_D_SDA	AA16	3.3V	I/O		I ² C channel D Data
51	GND					
52	DAC_A	D6	1.8V	O		
53	N.C.	-				
54	DAC_B	D7	1.8V	O		
55	N.C.	-				
56	SPI_A_CS0#	Y15	1.8V	O		
57	GND					
58	SPI_A_SDI	U15	1.8V	I		
59	N.C.	-				

Pin	Signal	OSM PIN	Voltage	I/O	PU/PD	Description
60	SPI_A_SDO	V15	1.8V	O		
61	N.C.	-				
62	SPI_A_SCK	U16	1.8V	O		
63	GND					
64	SPI_B_CS0#	AA23	1.8V	O		
65	N.C.	-				
66	SPI_B_SDI	Y22	1.8V	I		
67	N.C.	-				
68	SPI_B_SDO	Y23	1.8V	O		
69	GND					
70	SPI_B_SCK	Y21	1.8V	O		
71	N.C.	-				
72	GND					
73	N.C.	-				
74	CSI_A_CLK_P	B4	MIPI CSI	O		Camera Serial Interface channel A clock positive
75	GND					
76	CSI_A_CLK_N	B3	MIPI CSI	O		Camera Serial Interface channel A clock negative
77	N.C.	-				
78	GND					
79	N.C.	-				
80	CSI_A_DATA0_P	B1	MIPI CSI	O		Camera Serial Interface channel A data 0 positive
81	GND					
82	CSI_A_DATA0_N	C1	MIPI CSI	O		Camera Serial Interface channel A data 0 negative
83	N.C.	-				
84	GND					
85	N.C.	-				
86	CSI_A_DATA1_P	A3	MIPI CSI	O		Camera Serial Interface channel A data 1 positive
87	GND					
88	CSI_A_DATA1_N	A2	MIPI CSI	O		Camera Serial Interface channel A data 1 negative
89	N.C.	-				
90	GND					
91	N.C.	-				
92	N.C.	-				
93	GND					
94	N.C.	-				
95	N.C.	-				

Pin	Signal	OSM PIN	Voltage	I/O	PU/PD	Description
96	GND					
97	N.C.	-				
98	N.C.	-				
99	GND					
100	N.C.	-				

Table 4: Connector J1

2.3 Connector J2

Pin	Signal	OSM Pin	Voltage	I/O	PU/PD	Description
1	ETH_TX_P	-	IEEE 802.3ab	O		
2	AUDIO_A_VCC	-	3.0V	I		Audio power (Audio Codec)
3	ETH_TX_N	-	IEEE 802.3ab	O		
4	AUDIO_A_GND	-		I		Audio ground (Audio Codec), do not connect system ground
5	ETH_RX_P	-	IEEE 802.3ab	I		
6	AUDIO_A_LOUT_L	-		I		Audio channel A line out left (Audio Codec)
7	ETH_RX_N	-	IEEE 802.3ab	I		
8	AUDIO_A_LOUT_R	-		I		Audio channel A line out right (Audio Codec)
9	N.C.	-				
10	AUDIO_A_MIC	-		O		Audio channel A microphone (Audio Codec)
11	N.C.	-				
12	AUDIO_A_LIN_L	-		O		Audio channel A Line In Left (Audio Codec)
13	N.C.	-				
14	AUDIO_A_LIN_R	-		O		Audio channel A line in right (Audio Codec)
15	N.C.	-				
16	GND					
17	ETH_A_LED	-	3.3V	O		ETH channel A LED signal (Ethernet phy)
18	AUDIO_A_HP_L	-		O		Audio channel A headphone left (Audio Codec)
19	GND					
20	AUDIO_A_HP_R	-		O		Audio channel A headphone right (Audio Codec)
21	N.C.	-				
22	AUDIO_A_HP_GND	-		I		Audio channel A headphone ground (Audio Codec) Do not connect to system ground
23	N.C.	-				
24	VDD_5V0	VCC_IN	5.0V	I		Power Input
25	N.C.	-				
26	VDD_5V0	VCC_IN	5.0V	I		Power Input
27	N.C.	-				
28	VDD_5V0	VCC_IN	5.0V	I		Power Input
29	N.C.	-				
30	GND					
31	N.C.	-				
32	GND					

Pin	Signal	OSM Pin	Voltage	I/O	PU/PD	Description
33	N.C.	-				
34	GND					
35	N.C.	-				
36	VDD_VBAT	W17	3.3V	I		Connect Battery or 3.3V for Real Time Clock
37	N.C.	-				
38	N.C.	-				
39	GND					
40	VDD_3V3	-	3.3V	O		3.3V power output (max. 1A)
41	USB_HOST_VBUS	AB20	5V	I		USB Host power detection
42	RESET_IN#	U17		I		Reset input, low active
43	USB_HOST_D_P	AC22	USB	I/O		USB differential data pairs for port B
44	CARRIER_PWR_EN#	V17	3.3V	O	PU 10.0K	Carrier power enable signal, low active
45	USB_HOST_D_N	AB23	USB	I/O		USB differential data pairs for port B
46	N.C.	-				
47	USB_HOST_EN	AC20	3.3V	O	PU 2.2K	Power enable for USB VBUS voltage
48	ON_OFF#	AA9	1.8V	I	PU 10.0K	ON / OFF signal, low active
49	GND					
50	BOOTSEL#	T17	1.8V	I		Bootselect signal, low active
51	USB_OTG_VBUS	AB16	5V	O		USB port A port power detection
52	SD_A_VCC	C20	1.8V / 3.3V	I		SDIO A voltage level. Connect 1.8V or 3.3V
53	USB_OTG_EN	AV16	1.8V / 3.3V	O		USB OTG enable signal
54	N.C.	-				
55	USB_OTG_ID	AB14	1.8V	I		Input Contact to announce OTG device insertion on USB 2.0 port
56	SDIO_A_PWR_EN	D21	SDIO_A_VCC	O		SDIO A Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.
57	USB_OTG_D_P	AC14	USB	I/O		USB differential data pairs for port A
58	SDIO_A_WP	D20	SDIO_A_VCC	I		SDIO A Write Protect. This signal denotes the state of the write-protect tab on SD cards.
59	USB_OTG_D_N	AB13	USB	I/O		USB differential data pairs for port A
60	SDIO_A_CD#	J21	SDIO_A_VCC	I		SDIO A Card Detect. This signal indicates when a SDIO/MMC card is present.
61	GND					
62	SDIO_A_CMD	E20	SDIO_A_VCC	I/O		SDIO A Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.
63	PWM_1	F18	1.8V	O		Pulse width modulation 1
64	SDIO_A_CLK	F21	SDIO_A_VCC	O		SDIO A Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.

Pin	Signal	OSM Pin	Voltage	I/O	PU/PD	Description
65	GPIO_B_0	D19	1.8V	I/O		
66	SDIO_A_D0	G20	SD_A_VCC	I/O		SDIO A Data lines. These signals operate in push-pull mode.
67	GPIO_B_1	E19	1.8V	I/O		
68	SDIO_A_D1	G21	SD_A_VCC	I/O		SDIO A Data lines. These signals operate in push-pull mode.
69	GPIO_B_2	F19	1.8V	I/O		
70	SDIO_A_D2	H20	SD_A_VCC	I/O		SDIO A Data lines. These signals operate in push-pull mode.
71	GND					
72	SDIO_A_D3	H21	SD_A_VCC	I/O		SDIO A Data lines. These signals operate in push-pull mode.
73	PWM2	G18	1.8V	O		Pulse width modulation 2
74	SPI_A_WP	W16	1.8V	I/O		SPI A Write Protect
75	PWM3	H18	1.8V	O		Pulse width modulation 3
76	SPI_A_HOLD	W15	1.8V	I/O		SPI A Suspends Serial Input
77	GPIO_C_0	D3	1.8V / 3.3V	I/O		
78	SPI_A_CS1#	K17	1.8V			SPI A Master Chip Select 1
79	N.C.	-				
80	N.C.	-				
81	GND					
82	GND					
83	N.C.	-				
84	GPIO_A_1	E17	1.8V	I/O		
85	N.C.	-				
86	GPIO_A_2	F17	1.8V	I/O		
87	N.C.	-				
88	GPIO_A_3	G17	1.8V	I/O		
89	N.C.	-				
90	GPIO_A_4	H17	1.8V	I/O		
91	N.C.	-				
92	GPIO_A_5	J17	1.8V	I/O		
93	JTAG_TCK	N17	1.8V	I/O		Test Clock
94	N.C.	-				
95	JTAG_TMS	N19	1.8V	I/O		Test Mode Select
96	N.C.	-				
97	JTAG_TDI	P17	1.8V	I/O		Test Data Input
98	N.C.	-				

Pin	Signal	OSM Pin	Voltage	I/O	PU/PD	Description
99	JTAG_TDO	R17	1.8V	I/O		Test Data Output
100	N.C.	-				

Table 5: Connector J2

2.4 Ethernet

The module uses a KSZ8081 Ethernet PHY (Physical Layer Transceiver) which converts CPU RGMII Signals to standard Ethernet signals over twisted-pair copper cables (100BASE-TX, or 10BASE-T).

OSM Pin	OSM Signal	IC (conversion)	PicoCore™ Signal
J15	N.C	KSZ8081	ETH_TX_P
K16	ETH_A_(R)(G)MII_TX_EN(_ER)		ETH_TX_N
H15	ETH_A_(S)(R)(G)MII_TXD0		ETH_RX_P
G15	ETH_A_(S)(R)(G)MII_TXD1		ETH_RX_N
H16	N.C		
G16	N.C		
R15	ETH_A_(R)(G)MII_RX_CLK		
M15	ETH_A_(R)(G)MII_RX_DV(_ER)		
K15	ETH_A_(S)(R)(G)MII_RXD0		
L15	ETH_A_(S)(R)(G)MII_RXD1		-
N15	N.C		-
P15	N.C		-
T16	ETH_MDC		-
T15	ETH_MDIO		-

Table 6: Ethernet (100Mbit)

2.5 Audio

For audio, we use an audio codec that converts I²S digital audio signals into analog output. Control and configuration of the codec are handled via the I²C_D interface (OSM I²C_B).

OSM Pin	OSM Signal	IC (conversion)	PicoCore™ Signal
V21	I2S_A_DATA_IN	SGTL5000	AUDIO_A_MIC
W21	I2S_DATA_OUT		AUDIO_A_LIN_R
W18	I2S_LRCLK		AUDIO_A_LIN_L
W20	I2S_BITCLK		AUDIO_A_LOUT_R
V18	I2S_MCLK		AUDIO_A_LOUT_L
	-		AUDIO_A_HP_R
	-		AUDIO_A_HP_L

Table 7: Audio

2.6 Serial level shifter

Since the OSM module provides a 1.8 V TTL UART interface, we use a level shifter (TXB0108YZP) to translate the signal levels up to 3.3 V. The level shifter ensures that the OSM module is electrically compatible with the PicoCore™ standard.

2.7 Level shifter

TCA39306-Q1 is a level shifter specialized for I²C. OSM provides a 1.8V I²C (I2C_CAM_CLK / SDA) which is translated to a signal level of 3.3V

The LSF0204DRUTR level shifter is used for translating the CAN interface (1.8 V to 3.3 V). The level shifter ensures that the OSM module is electrically compatible with the PicoCore™ standard.

3 Characteristics

3.1 Absolute Maximum Ratings¹

Description	Min	Max	Unit
Supply Voltage	-0.50	6.00	V
Audio supply voltage	-0.30	3.60	V
Real Time Clock (RTC) supply voltage	-0.50	6.50	V

Table 8: Absolute maximum ratings

3.2 Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
General					
VDD_5V0	Module main supply voltage	4.50	5.00	5.50	V
AUDIO_A_VCC	Supply voltage for SGT15000	1.62	3.00	3.60	V
V_RTC	Real time clock voltage	Depends on OSM			
Analog Input / Output					
DAC0 & DAC1	DAC full scale output voltage range	Depends on OSM			

Table 9: Recommended operate conditions

¹ Stresses beyond the listed values may affect reliability or cause permanent damage to the module

4 Packaging & Labels

4.1 ESD

All F&S electrostatic discharge sensitive (ESD) products are marked and will be shipped in ESD protective packaging.

4.2 Serial Number

All shipped F&S products are labeled with a matrix code sticker that includes the serial number. For product information visit www.fsembedded.com/en/support/serial-number-info-and-rma/.

5 Appendix

5.1 Second source rules

The qualifications of products from a second source are done autonomously by F&S. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible. F&S does not use broker components without the consent of the customer.

5.2 RoHS and REACH statement

Please see the following webpage: www.fsembedded.com/en/support/certifications/

5.3 Important Notice

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Specifications are subject to change without notice.

6 Warranty Terms

6.1 Hardware Warranties

F&S guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and F&S's sole liability shall be for F&S, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

6.2 Software Warranties

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