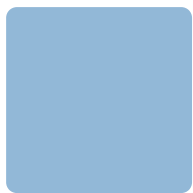


Hardware Documentation

ADP-OSM-BB *for HW Revision 1.30*

Version 002/07.2025

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**Elektronik
Systeme**

© F&S Elektronik Systeme GmbH
Untere Waldplätze 23
D-70569 Stuttgart

www.fseembedded.com

Phone: +49(0)711-123722-0

About This Document

This document describes how to use the ADP-OSMBB with mechanical and electrical information. The latest version of this document can be found at: www.fseembedded.com.

ESD Requirements



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History

Version	Date	Platform	Added (A) Removed (R) Modified (M)	Chapter	Description	Author
000/06.2024	03.07.2024	-	-	All	Initial Version	TM
002/07.2025	22.07.2025 3.07.2025	-	M	All	Updated template, new hardware revision	GI

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1 Overview

1.1 Additional Documentation

The latest versions of the documents can be found on www.fsembedded.com.

The Open Standard Module specification can be found [here](#)

1.2 Description

ADP-OSM-BB is a adapter solution to convert Open Standard Module™ (OSM) to PicoCore™ standard with PicoCore™ B2B connectors.

1.3 General Parameter

Parameter	Description
Dimension	35.0 mm x 40.0 mm x 4.60 mm
Weight	≈ 10.0 g (with mounted OSM93)
Operating Temperature	-40.0 °C ... +85.0 °C, also depending on OSM
Mounting Holes	2x Ø 2.3 mm

Table 1: General parameter

1.4 Dimensions and Connectors

1.4.1 Technical Drawing

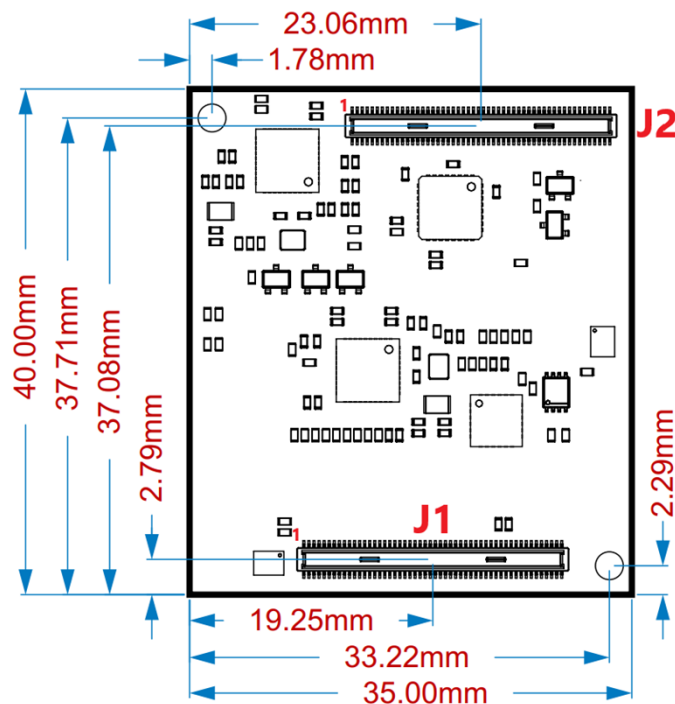


Figure 1: Technical drawing (view from bottom)

1.4.2 Connectors¹

Ref.	Description	Connector Type	Counter Part
J1	Board to board connector	DF40C-100DP-0.4V(51)	DF40C-100DS-0.4V(51)
J2	Board to board connector	DF40C-100DP-0.4V(51)	DF40C-100DS-0.4V(51)

¹Connectors and preassembled cables are available for purchase at www.fsembedded.com.

Table 2: Connector description

2 Connector Signal Description

2.1 Contact type definition

Contact Type	Description
I	Input to the module
O	Output from the module
I/O	Bi-directional input / output signal
N.C.	Not connected
PU	Pull up resistor
PD	Pull down resistor

Table 3: Contact Types

2.2 B2B J1 (Serial, SPI, CAN, I²C, MIPI-CSI&DSI, mPCIe)

The following table shows the contact signal description of the board to board connectors

Pin	Signal	OSM PIN	Voltage	I/O	PU/PD	Description
1	I2C_CAM_IRQ	D17	3.3V	I		I ² C interrupt
2	!TOUCH_RESET	-	3.3V	O		Signal from I/O expander, low active
3	I2C_CAM_CLK	C4	3.3V	I/O	PU 2.2K	I ² C Clock
4	I2C_A_SCL	AA15	1.8V	I/O		I ² C channel A Clock
5	I2C_CAM_SDA	C3	3.3V	I/O	PU 2.2K	I ² C Data
6	I2C_A_SDA	AA16	1.8V	I/O		I ² C channel A Data
7	!MIPI_RESET	-	3.3V	O		Signal from I/O expander, low active
8	GND					
9	BL_ON	-	3.3V	O		Backlight ON, Signal from I/O expander
10	CAN_A_RX	AB17	3.3V	O		CAN channel A receive
11	BL_PWM	E18	3.3V	O		Backlight PWM
12	CAN_A_TX	AC17	3.3V	I		CAN channel A Transmit
13	VLCD_ON	-	3.3V	O		Power Enable for display, Signal from I/O expander
14	N.C.	-				
15	GND					
16	N.C.	-				
17	DSI_A_CLK_P	AB7	MIPI DSI	O		Display Serial Interface Clock positive
18	UART_A_RXD	D22	3.3V	O		RS232 channel A receive
19	DSI_A_CLK_N	AB8	MIPI DSI	O		Display Serial Interface Clock negative
20	UART_A_TXD	D23	3.3V	I		RS232 channel A transmit
21	GND					
22	UART_B_RTS	D15	3.3V	O		RS232 channel B ready to send
23	DSI_A_DATA0_P	AB10	MIPI DSI	O		Display Serial Interface Data 0 positive

Pin	Signal	OSM PIN	Voltage	I/O	PU/PD	Description
24	UART_B_CTS	C14	3.3V	O		RS232 channel B clear to send
25	DSI_A_DATA0_N	AB11	MIPI DSI	O		Display Serial Interface Data 0 negative
26	UART_B_RXD	D14	3.3V	O		RS232 channel B receive
27	GND					
28	UART_B_TXD	D13	3.3V	I		RS232 channel B transmit
29	DSI_A_DATA1_P	AC8	MIPI DSI	O		Display Serial Interface Data 1 positive
30	N.C.	-				
31	DSI_A_DATA1_N	AC9	MIPI DSI	O		Display Serial Interface Data 1 negative
32	N.C.	-				
33	GND					
34	UART_D_RXD	A22	3.3V	O		RS232 channel D receive
35	DSI_A_DATA2_P	AC5	MIPI DSI	O		Display Serial Interface Data 2 positive
36	UART_D_TXD	B23	3.3V	I		RS232 channel D transmit
37	DSI_A_DATA2_N	AC6	MIPI DSI	O		Display Serial Interface Data 2 negative
38	GND					
39	GND					
40	MPCIE_SMCLK	T1	1.8V	I/O		PCIe system management I ² C Clock
41	DSI_A_DATA3_P	AB4	MIPI DSI	O		Display Serial Interface Data 3 positive
42	MPCIE_SMDAT	U1	1.8V	I/O		PCIe system management I ² C Data
43	DSI_A_DATA3_N	AB5	MIPI DSI	O		Display Serial Interface Data 3 negative
44	GPIO_J1_44	-	3.3V	I/O		Signal from I/O expander
45	GND					
46	GPIO_J1_46	-	3.3V	I/O		Signal from I/O expander
47	N.C.	-				
48	I2C_D_SCL	AA15	3.3V	I/O		I ² C channel D Clock
49	N.C.	-				
50	I2C_D_SDA	AA16	3.3V	I/O		I ² C channel D Data
51	GND					
52	N.C.	-				
53	N.C.	-				
54	N.C.	-				
55	N.C.	-				
56	SPI_B_SS0	AA23	1.8V	O		SPI channel B master chip select 0
57	GND					
58	SPI_B_MISO	Y22	1.8V	I		SPI channel B master in slave out
59	N.C.	-				

Pin	Signal	OSM PIN	Voltage	I/O	PU/PD	Description
60	SPI_B_MOSI	Y23	1.8V	O		SPI channel B master out slave in
61	N.C.	-				
62	SPI_B_SCLK	Y21	1.8V	O		SPI channel B Clock
63	GND					
64	SPI_A_SS0	Y15	1.8V	O		SPI channel A master chip select 0
65	N.C.	-				
66	SPI_A_MISO	V15 / U15	1.8V	I		SPI channel A master in slave out, exchangeable with J1 68 SPI_A_MOSI via jumper
67	N.C.	-				
68	SPI_A_MOSI	V15 / U15	1.8V	O		SPI channel A master out slave in, exchangeable with J1 66 SPI_A_MISO via jumper
69	GND					
70	SPI_A_SCLK	U16	1.8V	O		SPI channel A Clock
71	N.C.	-				
72	GND					
73	N.C.	-				
74	CSI_A_CLK_P	B4	MIPI CSI	O		Camera Serial Interface channel A clock positive
75	GND					
76	CSI_A_CLK_N	B3	MIPI CSI	O		Camera Serial Interface channel A clock negative
77	MPCIE_CTX_P	AC2	mPCle	I		mPCle transmit positive
78	GND					
79	MPCIE_CTX_N	AC3	mPCle	I		mPCle transmit negative
80	CSI_A_DATA0_P	B1	MIPI CSI	O		Camera Serial Interface channel A data 0 positive
81	GND					
82	CSI_A_DATA0_N	C1	MIPI CSI	O		Camera Serial Interface channel A data 0 negative
83	MPCIE_CRX_P	AB1	mPCle	O		mPCle receive positive
84	GND					
85	MPCIE_CRX_N	AB2	mPCle	O		PCle receive negative
86	CSI_A_DATA1_P	A3	MIPI CSI	O		Camera Serial Interface channel A data 1 positive
87	GND					
88	CSI_A_DATA1_N	A2	MIPI CSI	O		Camera Serial Interface channel A data 1 negative
89	MPCIE_CLK_P	W1	mPCle	I		mPCle clock positive
90	GND					
91	MPCIE_CLK_N	Y1	mPCle	I		mPCle clock negative
92	CSI_A_DATA2_P	A6	MIPI CSI	O		Camera Serial Interface channel A data 2 positive
93	GND					
94	CSI_A_DATA2_N	A5	MIPI CSI	O		Camera Serial Interface channel A data 2 negative

Pin	Signal	OSM PIN	Voltage	I/O	PU/PD	Description
95	MPCIE_PERST	V2	1.8V	O		mPCle reset signal
96	GND					
97	MPCIE_WAKE	T2	1.8V	O		mPCle wake signal
98	CSI_A_DATA3_P	B7	MIPI CSI	O		Camera Serial Interface channel A data 3 positive
99	GND					
100	CSI_A_DATA3_N	B6	MIPI CSI	O		Camera Serial Interface channel A data 3 negative

Table 4: Pinout J1

2.3 B2B J2 (Audio, USB OTG, USB Host, Ethernet A, Ethernet B, SD Card, ADC)

Pin	Signal	OSM Pin	Voltage	I/O	PU/PD	Description
1	ETH_A_D1_P	ETH_A	IEEE 802.3ab	I/O		Ethernet channel A data 1 positive (Ethernet Phy Gbit)
2	AUDIO_A_VCC	-	3.0V	I		Audio power (Audio Codec)
3	ETH_A_D1_N	ETH_A	IEEE 802.3ab	I/O		Ethernet channel A data 1 negative (Ethernet Phy)
4	AUDIO_A_GND	-		I		Audio ground (Audio Codec), do not connect system ground
5	ETH_A_D2_P	ETH_A	IEEE 802.3ab	I/O		Ethernet channel A data 2 positive (Ethernet Phy)
6	AUDIO_A_LOUT_L	I ² S_A		I		Audio channel A Line Out Left (Audio Codec)
7	ETH_A_D2_N	ETH_A	IEEE 802.3ab	I/O		Ethernet channel A data 2 negative (Ethernet Phy)
8	AUDIO_A_LOUT_R	I ² S_A		I		Audio channel A Line Out Right (Audio Codec)
9	ETH_A_D3_P	ETH_A	IEEE 802.3ab	I/O		Ethernet channel A data 3 positive (Ethernet Phy)
10	AUDIO_A_MIC	I ² S_A		O		Audio channel A microphone (Audio Codec)
11	ETH_A_D3_N	ETH_A	IEEE 802.3ab	I/O		Ethernet channel A data 3 negative (Ethernet Phy)
12	AUDIO_A_LIN_L	I ² S_A		O		Audio channel A Line In Left (Audio Codec)
13	ETH_A_D4_P	ETH_A	IEEE 802.3ab	I/O		Ethernet channel A data 4 positive (Ethernet Phy)
14	AUDIO_A_LIN_R	I ² S_A		O		Audio channel A Line In Right (Audio Codec)
15	ETH_A_D4_N	ETH_A	IEEE 802.3ab	I/O		Ethernet channel A data 4 negative (Ethernet Phy)
16	GND					
17	ETH_A_LED	-	3.3V	O		ETH channel A LED Signal (Ethernet Phy)
18	AUDIO_A_HP_L	I ² S_A		O		Audio channel A Headphone Left (Audio Codec)
19	GND					
20	AUDIO_A_HP_R	I ² S_A		O		Audio channel A Headphone Right (Audio Codec)
21	ETH_B_LED	ETH_B	3.3V	O		ETH channel B LED Signal (Ethernet Phy)
22	AUDIO_A_HP_GND	-		I		Audio channel A Headphone Ground (Audio Codec) Do not connect to system ground

Pin	Signal	OSM Pin	Voltage	I/O	PU/PD	Description
23	ETH_B_D1_P	ETH_B	IEEE 802.3ab	I/O		Ethernet channel B data 1 positive (Ethernet Phy)
24	VDD_5V0	VCC_IN	5.0V	I		Power Input
25	ETH_B_D1_N	ETH_B	IEEE 802.3ab	I/O		Ethernet channel B data 1 negative (Ethernet Phy)
26	VDD_5V0	VCC_IN	5.0V	I		Power Input
27	ETH_B_D2_P	ETH_B	IEEE 802.3ab	I/O		Ethernet channel B data 2 positive (Ethernet Phy)
28	VDD_5V0	VCC_IN	5.0V	I		Power Input
29	ETH_B_D2_N	ETH_B	IEEE 802.3ab	I/O		Ethernet channel B data 2 negative (Ethernet Phy)
30	GND					
31	ETH_B_D3_P	ETH_B	IEEE 802.3ab	I/O		Ethernet channel B data 3 positive (Ethernet Phy)
32	GND					
33	ETH_B_D3_N	ETH_B	IEEE 802.3ab	I/O		Ethernet channel B data 3 negative (Ethernet Phy)
34	GND					
35	ETH_B_D4_P	ETH_B	IEEE 802.3ab	I/O		Ethernet channel B data 4 positive (Ethernet Phy)
36	VDD_VBAT	W17	3.3V	I		Connect Battery or 3.3V for Real Time Clock
37	ETH_B_D4_N	ETH_B	IEEE 802.3ab	I/O		Ethernet channel B data 4 negative (Ethernet Phy)
38	N.C.	-				
39	GND					
40	VDD_3V3	-	3.3V	O		3.3V power output (max. 1A)
41	USB_HOST_VBUS	AB20	5V	O		USB Host power delivery
42	!RESET_IN	U17		I	PU 10.0K	Reset input, low active
43	USB_HOST_D_P	AC22	I/O USB	I/O		USB Host data positive
44	!CARRIER_PWR_EN	V17	3.3V	O	PU 10.0K	Carrier power enable signal, low active
45	USB_HOST_D_N	AB23	I/O USB	I/O		USB Host data negative
46	N.C.	-				
47	USB_HOST_EN	AC20	3.3V	O		USB Host enable
48	!ON_OFF	AA9	1.8V	I	PU 10.0K	ON / OFF signal, low active
49	GND					
50	!BOOTSEL	T17	1.8V	I	PU 10.0K	Bootselect signal, low active
51	USB_OTG_VBUS	AB16	5V	O		USB OTG power delivery
52	SD_A_VCC	C20	1.8V / 3.3V	I		SDIO A voltage level. Connect 1.8V or 3.3V
53	USB_OTG_EN	AV16	1.8V / 3.3V	O		USB OTG enable signal
54	N.C.	-				

Pin	Signal	OSM Pin	Voltage	I/O	PU/PD	Description
55	USB_OTG_ID	AB14		O	PU 10.0K	USB OTG ID signal (connect PU / PD)
56	SD_A_RST	D21	SD_A_VCC	O		SD Card reset signal
57	USB_OTG_D_P	AC14	USB2.0	I/O		USB OTG data positive
58	SD_A_WP	D20	SD_A_VCC	O		SD Card write protect signal
59	USB_OTG_D_N	AB13	USB2.0	I/O		USB OTG data negative
60	SD_A_CD	J21	SD_A_VCC	I		SD Card Card Detect signal
61	GND					
62	SD_A_CMD	E20	SD_A_VCC	O		SD Card command
63	PWM	F18	1.8V	O		PWM output signal
64	SD_A_CLK	F21	SD_A_VCC	O		SD Card clock
65	N.C.	-				
66	SD_A_DATA0	G20	SD_A_VCC	I/O		SD Card Data 0
67	N.C.	-				
68	SD_A_DATA1	G21	SD_A_VCC	I/O		SD Card Data 1
69	N.C.	-				
70	SD_A_DATA2	H20	SD_A_VCC	I/O		SD Card Data 2
71	GND					
72	SD_A_DATA3	H21	SD_A_VCC	I/O		SD Card Data 3
73	ADC0	M18	0 – 1.8V	I		Analog Digital Converter input 0
74	N.C.	-				
75	ADC1	N18	0 – 1.8V	I		Analog Digital Converter input 1
76	N.C.	-				
77	!USB_TYPEC_ALERT	-	3.3V			Signal from I/O expander, low active
78	N.C.	-				
79	N.C.	-				
80	N.C.	-				
81	GND					
82	GND					
83	N.C.	-				
84	N.C.	-				
85	N.C.	-				
86	N.C.	-				

Pin	Signal	OSM Pin	Voltage	I/O	PU/PD	Description
87	N.C.	-				
88	N.C.	-				
89	N.C.	-				
90	N.C.	-				
91	N.C.	-				
92	N.C.	-				
93	JTAG_TCK	N17	1.8V	I/O		JTAG Clock
94	N.C.	-				
95	JTAG_TMS	N19	1.8V	I/O		JTAG Mode Select
96	N.C.	-				
97	JTAG_TDI	P17	1.8V	I/O		JTAG Data In
98	N.C.	-				
99	JTAG_TDO	R17	1.8V	I/O		JTAG Data Out
100	N.C.	-				

Table 5: Pinout J2

3 Detailed Description

3.1 Ethernet

The module uses 2 RTL8211 Ethernet PHYs (Physical Layer Transceiver) which converts CPU RGMII Signals to standard Ethernet signals over twisted-pair copper cables (1000BASE-T, 100BASE-TX, or 10BASE-T).

OSM Pin	OSM Signal	IC (conversion)	PicoCore™ Signal
J15	ETH_A_(R)(G)MII_TX_CLK	RTL8211	ETH_A_D1_P
K16	ETH_A_(R)(G)MII_TX_EN(_ER)		ETH_A_D1_N
H15	ETH_A_(S)(R)(G)MII_TXD0		ETH_A_D2_P
G15	ETH_A_(S)(R)(G)MII_TXD1		ETH_A_D2_N
H16	ETH_A_(S)(R)(G)MII_TXD2		ETH_A_D3_P
G16	ETH_A_(S)(R)(G)MII_TXD3		ETH_A_D3_N
R15	ETH_A_(R)(G)MII_RX_CLK		ETH_A_D4_P
M15	ETH_A_(R)(G)MII_RX_DV(_ER)		ETH_A_D4_N
K15	ETH_A_(S)(R)(G)MII_RXD0		ETH_A_LED
L15	ETH_A_(S)(R)(G)MII_RXD1		-
N15	ETH_A_(R)(G)MII_RXD2		-
P15	ETH_A_(R)(G)MII_RXD3		-
T16	ETH_A_MDC		-
T15	ETH_A_MDIO		-

Table 6: Ethernet A (Gbit) used OSM Pins

OSM Pin	OSM Signal	IC (conversion)	PicoCore™ Signal
H1	ETH_B_(R)(G)MII_TX_CLK	RTL8211	ETH_B_D1_P
J2	ETH_B_(R)(G)MII_TX_EN(_ER)		ETH_B_D1_N
G1	ETH_B_(S)(R)(G)MII_TXD0		ETH_B_D2_P
F1	ETH_B_(S)(R)(G)MII_TXD1		ETH_B_D2_N
G2	ETH_B_(S)(R)(G)MII_TXD2		ETH_B_D3_P
F2	ETH_B_(S)(R)(G)MII_TXD3		ETH_B_D3_N
P1	ETH_B_(R)(G)MII_RX_CLK		ETH_B_D4_P
L1	ETH_B_(R)(G)MII_RX_DV(_ER)		ETH_B_D4_N
J1	ETH_B_(S)(R)(G)MII_RXD0		ETH_B_LED
K1	ETH_B_(S)(R)(G)MII_RXD1		-
M1	ETH_B_(R)(G)MII_RXD2		-
N1	ETH_B_(R)(G)MII_RXD3		-
C6	ETH_B_MDC		-
C7	ETH_B_MDIO		-

Table 7: Ethernet B (Gbit) used OSM Pins

3.2 I/O Expander

To reach the required number of GPIOs, 1 GPIO expander is used (PCAL6416A).

This expander can be accessed over I²C Channel D (OSM I²C_B) (write 0x40, read 0x41)

It provides following I/Os

Pin	Signal	Voltage	I/O	PU/PD	Description
1	!PHY_RST_A	3.3V	O	PU 10.0K	Low active, necessity for ETH RTL8211
2	!PHY_RST_B	3.3V	O	PU 10.0K	Low active, necessity for ETH RTL8211
3	!PHY_IRQ_A	3.3V	I	PU 10.0K	Low active, necessity for ETH RTL8211
4	PHY_IRQ_B	3.3V	I	PU 10.0K	Low active, necessity for ETH RTL8211
5	!USB_TYPEC_ALERT		I		Low active, required for USB alert
6	!MIPI_RESET		O		Low active, MIPI display reset
7	!TOUCH_RESET		O		Low active, touch reset
8	BL_ON	3.3V	O		Backlight on signal (default: from I/O expander, OSM otherwise)
10	VLCD_ON	3.3V	O		Display power on signal (default: from I/O expander, OSM otherwise)
11	GPIO_J1_44	3.3V	I/O		General Purpose Input/Output
12	GPIO_J1_46	3.3V	I/O		General Purpose Input/Output

Table 8: I/O expander (PCAL6416A)

Note: PCAL6416A uses OSM AA20 I²C_B_SCL , AA21 I²C_B_SDA and E17 GPIO_A_1 for full functionality

3.3 Serial level shifter

Since the OSM module provides a 1.8 V TTL UART interface, we use a level shifter (TXB0108YZP) to translate the signal levels up to 3.3 V. The level shifter ensures that the OSM module is electrically compatible with the PicoCore™ standard.

3.4 Level shifter

TCA39306-Q1 is a level shifter specialized for I²C. OSM provides a 1.8V I²C (I2C_CAM_CLK / SDA) which is translated to a signal level of 3.3V

The second level shifter is used for translating the CAN interface (1.8 V to 3.3 V) as well as the control signals BL_ON, BL_PWM, and VLCD_ON. The level shifter ensures that the OSM module is electrically compatible with the PicoCore™ standard.

3.5 Audio

For audio, we use an audio codec that converts I²S digital audio signals into analog output. Control and configuration of the codec are handled via the I²C_D interface (OSM I²C_B).

OSM Pin	OSM Signal	IC (conversion)	PicoCore™ Signal
V21	I2S_A_DATA_IN	SGTL5000	AUDIO_A_MIC
W21	I2S_DATA_OUT		AUDIO_A_LIN_R
W18	I2S_LRCLK		AUDIO_A_LIN_L
W20	I2S_BITCLK		AUDIO_A_LOUT_R
V18	I2S_MCLK		AUDIO_A_LOUT_L
	-		AUDIO_A_HP_R
	-		AUDIO_A_HP_L
	-		

4 Characteristics

4.1 Absolute Maximum Ratings¹

Description	Min	Max	Unit
Supply Voltage	-0.50	6.00	V
Audio supply voltage	-0.30	3.60	V
Real Time Clock (RTC) supply voltage	-0.50	6.50	V

Table 9: Absolute maximum ratings

4.2 Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
General					
VDD_5V0	Module main supply voltage	4.50	5.00	5.50	V
AUDIO_A_VCC	Supply voltage for SGT15000	1.62	3.00	3.60	V
V_RTC	Real time clock voltage	Depends on OSM			
Analog Input / Output					
ADC0 & ADC1	ADC full scale input voltage range	Depends on OSM			

Table 10: Recommended operate conditions

¹ Stresses beyond the listed values may affect reliability or cause permanent damage to the module

5 Packaging & Labels

5.1 ESD

All F&S electrostatic discharge sensitive (ESDS) products are marked and will be shipped in ESD protective packaging.

5.2 Serial Number

All shipped F&S products are labeled with a matrix code sticker that includes the serial number. For product information visit www.fsembedded.com/en/support/serial-number-info-and-rma/.

6 Appendix

6.1 Second source rules

The qualifications of products from a second source are done autonomously by F&S. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible. F&S does not use broker components without the consent of the customer.

6.2 RoHS and REACH statement

Please see the following webpage: www.fsembedded.com/en/support/certifications/

6.3 Important Notice

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7 Warranty Terms

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