Hardware Documentation

PicoCoreMX8ULP

for HW Revision 1.30

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About This Document

This document describes how to use the PicoCoreMX8ULP (further named as module) with mechanical and electrical information. The latest version of this document can be found at: www.fsembedded.com.

ESD Requirements

All F&S hardware products are electrostatic discharge (ESD) sensitive. All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD sensitive material in ESD unsafe environments. Negligent handling will harm the product and warranty claims become void.

Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

History

Version	Date	Platform	Added (A) Removed (R) Modified (M)	Chapter	Description	Author
001/10.2025	21.10.2025	-	-	All	Initial Version	SM
002/02.2026	26.02.2026	-	 M M M M M M	2.1, 2.2.7, 3 1.4.3, 2.1.4 1.4.3, 2.1.4 2.2.12 2.2.3 2.2.3	Update to Rev. 1.30 Add reference voltage for analog signals Remove PMIC_ON_REQ from B2B Con. Remove PMIC_STBY_REQ from B2B Con. Added PU to USB_OTG_ID Inverted ETH_LED Logic Exchange internal pad of J2.35 & J2.37	SM
003/04.2026	21.04.20261 3.05.2026	-	M	1.4.3, 2.1.3, 3.2	Fig. 3, 4 & 5 have been replaced with the actual versions. Information regarding $I_{5V0,max}$ corrected.	UK
004/05.2026	11.05.2026	-	M	2.1.4	Note regarding BOOTSEL-pin added.	UK

Table of Content

Tables

Figures

1 Overview

1.1 Additional Documentation

The latest versions of the documents can be found on www.fsembedded.com.

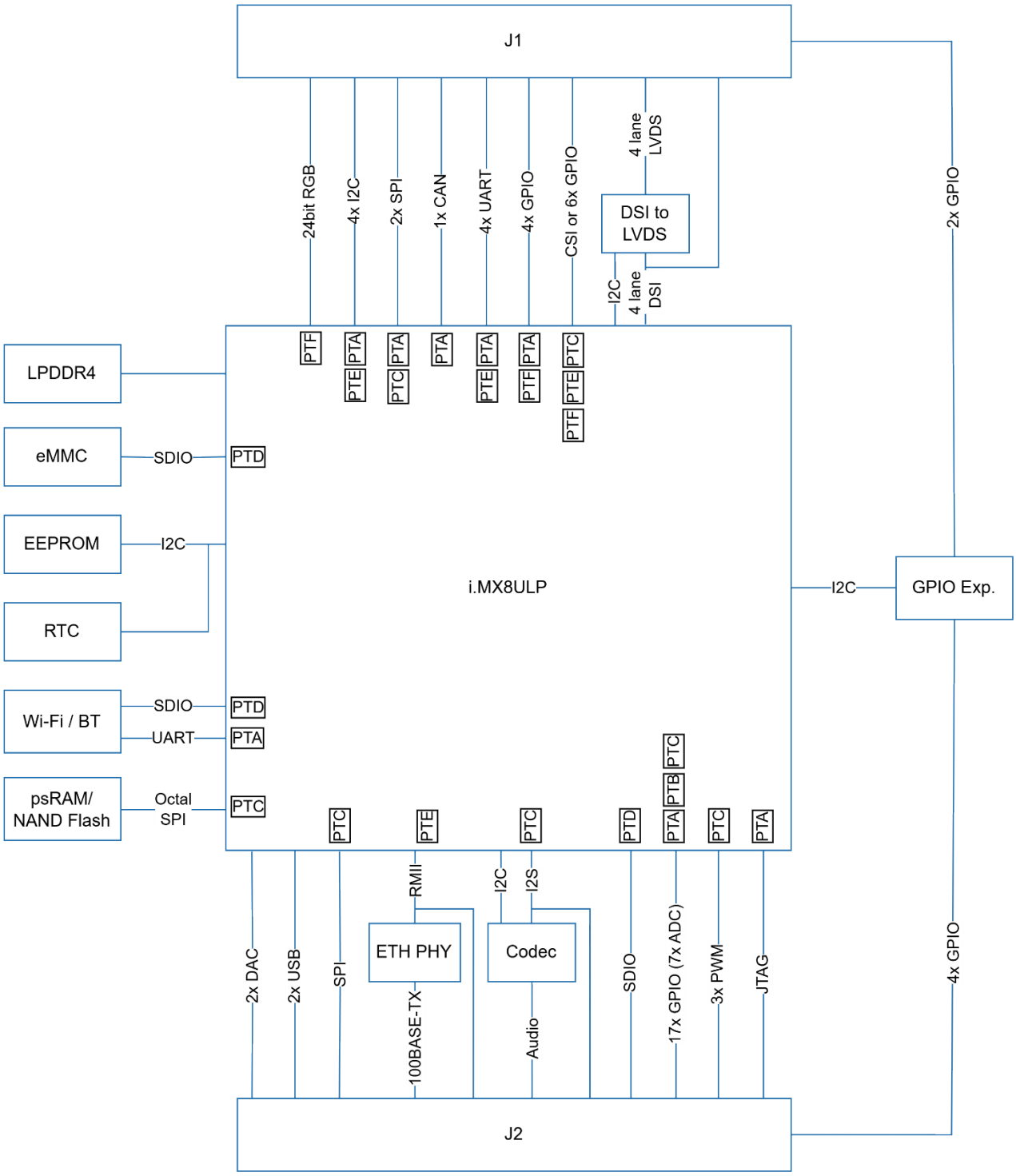
1.2 General Parameter

Parameter	Description
Dimension	40.0 mm x 35.0 mm x 4.2 mm
Weight	≈ 15.0g
Operating Temperature	-40.0 °C … +85.0 °C
Mounting Holes	2x Ø 2.3 mm
Pin Count	200

Table 1: General Parameter

1.3 Block Diagram

The following figure shows the intended functionalities of the module.



Note: The availability depends on the configuration.

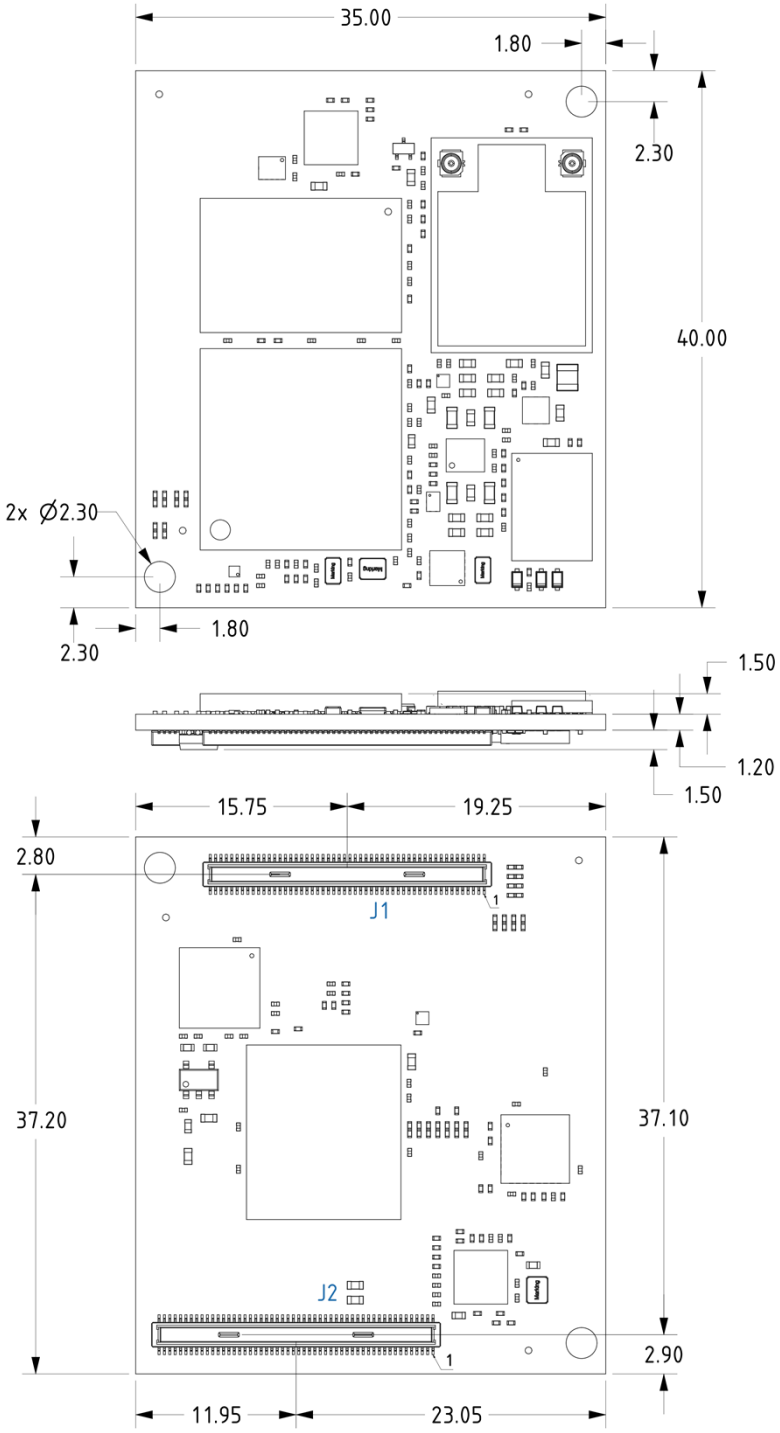
Figure 1: Block Diagramm

Additionally, F&S supports customized solutions with a different IOMUX.

Note: This may lead to completely different configurations. Please contact sales@fs-net.de for further information.

1.4 Dimensions and Connectors

1.4.1 Technical Drawing



Note: All dimensions are in mm.

Figure 2: Technical Drawing

1.4.2 Connectors

Ref.	Description	Connector Type	Counter Part
J1	Board to Board Connector	Hirose, DF40C-100DP-0.4V	Hirose, DF40C-100DS-0.4V[1]
J2			

[1]Connectors and preassembled cables are available for purchase at www.fsembedded.com.

Table 2: Connector Description

1.4.3 Connector Schematic

The following figures show an overview of the board-to-board connectors and the associated signals.

The contact names refer to our PicoCore default description. To simplify the representation, the contact names describe only the primary function. Therefore, the actual function can be differed from that name.

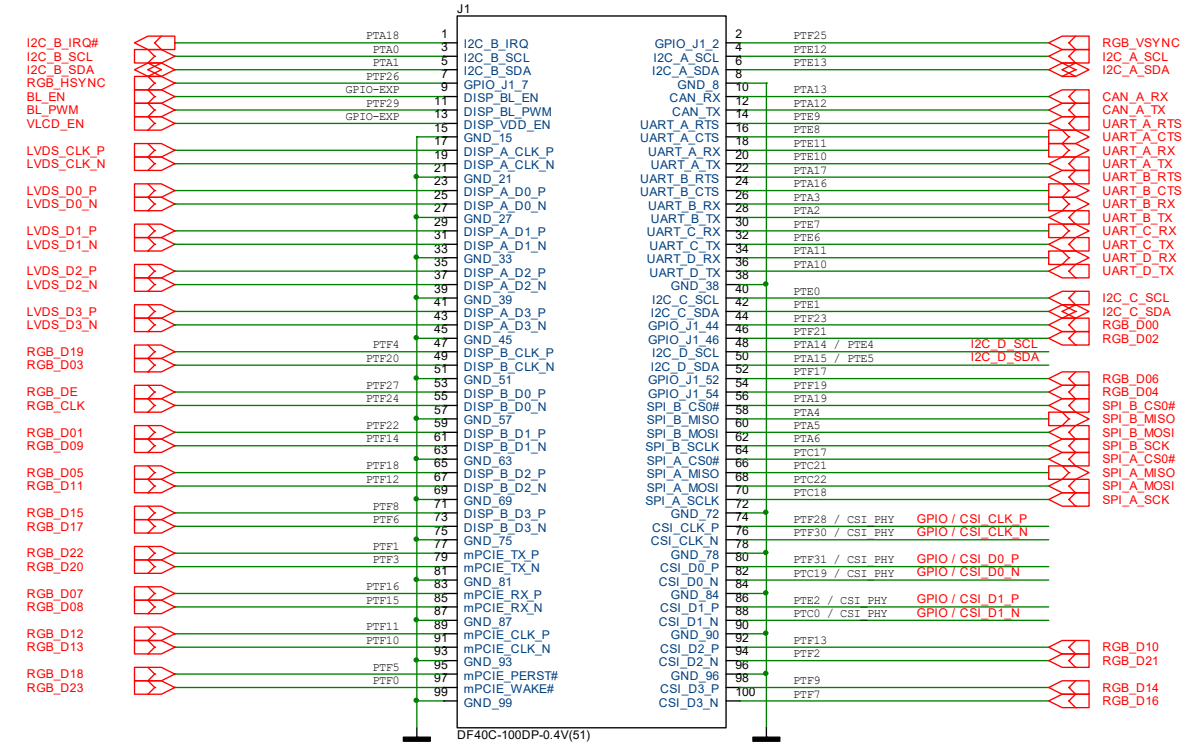


Figure 3: B2B J1 (schematic)

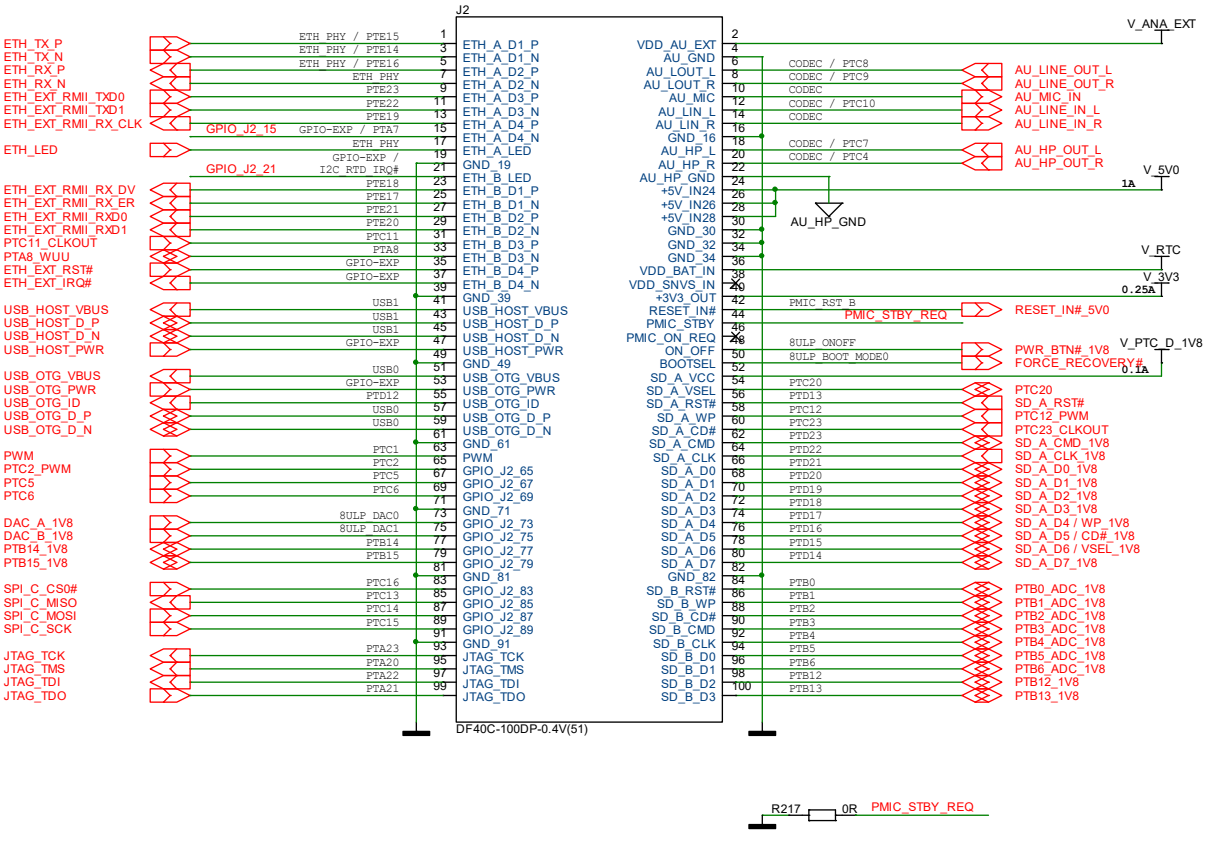


Figure 4: B2B J2 (schematic)

2 Detailed Description

2.1 Power Management

2.1.1 Power Supply

The following table shows the intended use of the power (PWR) pins on the module.

Ref.	Pin	Contact Name	Voltage	I/O	Description
J1	8,15,21,23,27,33,38,39,45, 51,57,63,69,72,75,78,81, 84,87,90,93,96,99	GND			
J2	24,26,28	V_5V0	5.0 V	PI	Main supply voltage
	36	VDD_BAT_IN	3.0 V	PI	Real time clock (RTC) supply input[1]
	40	+3V3_OUT	3.3 V	PO	Supply for peripherals or as reference, max.: 250 mA
	52	SD_A_VCC	1.8 V	PO	Supply and reference voltage for SDIO port A,max.: 100 mA
	2	V_AU_EXT	1.8V / 3.3V	PI	Optional external analog supply for audio (V_AU_VDDA) or analog signals [2]
	4	AU_GND	Audio ground for LINE IN & Out		
	22	HP_GND	Headphone ground		
	16,19,30,32,34, 39,49,61,71,81, 82,91	GND			

Table 3: Power Supply (pin description)

[1] VDD_BAT_IN may be sourced from a Carrier based Li-cell or Super Cap.

[2] mounting option

2.1.2 Erratum ERR052513: Parametric Shift on FSGPIO Output Driver

According to iMX8ULPA2_P40A (Mask Set Errata), Erratum ERR052513, NXP observed a parametric shift over time on the FSGPIO (Fail-Safe GPIO) output drivers of PTA, PTE & PTF when the IO bank is supplied by voltages above 1.98 V.

This shift only impacts the pin output driver capability and does not impact the pin analog or pin digital input functionality.

Note: In TN00188 (FSGPIO Failure Risk Assessment), NXP states that the parametric shift can be represented by a reduced output driving capability of the low-side transistor of the output driver (NMOS). The degraded output low drive current (IOL) leads to a longer fall time t_F and an increased output low voltage level (VOL). In addition, NXP describes six factors that have an impact on the speed of the degradation:

- I/O bank supply voltage (a lower voltage significantly reduces the speed of degradation)
- Signal toggling frequency (a higher frequency represents a faster degradation)
- Toggle rate (a higher toggle rate represents a faster degradation)
- Temperature (a lower effective junction temperature represents a faster degradation)
- Pin output driver configuration (slower degradation with a high drive strength and standard slew rate configuration)
- Loading capacitance (should be minimized)

For an assessment of whether this Erratum has an impact on a specific application, TN00188 contains a failure analysis and tables with estimated worst case IOL values as a function of the above parameters for different mission profiles. The latest versions of the documents

- iMX8ULPA2_P40A Mask Set Errata,
- TN00188 FSGPIO Failure Risk Assessment (login required)

can be downloaded from the NXP website.

The NXP FSGPIO failure analysis shows that lowering the I/O bank supply voltage is a very effective approach to slow down the parametric shift over time. The module contains an adjustable DC/DC converter which generates the general 3.3 V supply voltage V_3V3 that may be lowered to V_3V3_{min} = 3.0 V (mounting option), if needed.

Peripherals on the carrier may be supplied with V_3V3 and up to 0.25 A by the module.

2.1.3 Power Topology

The following picture visualizes the power topology of the module

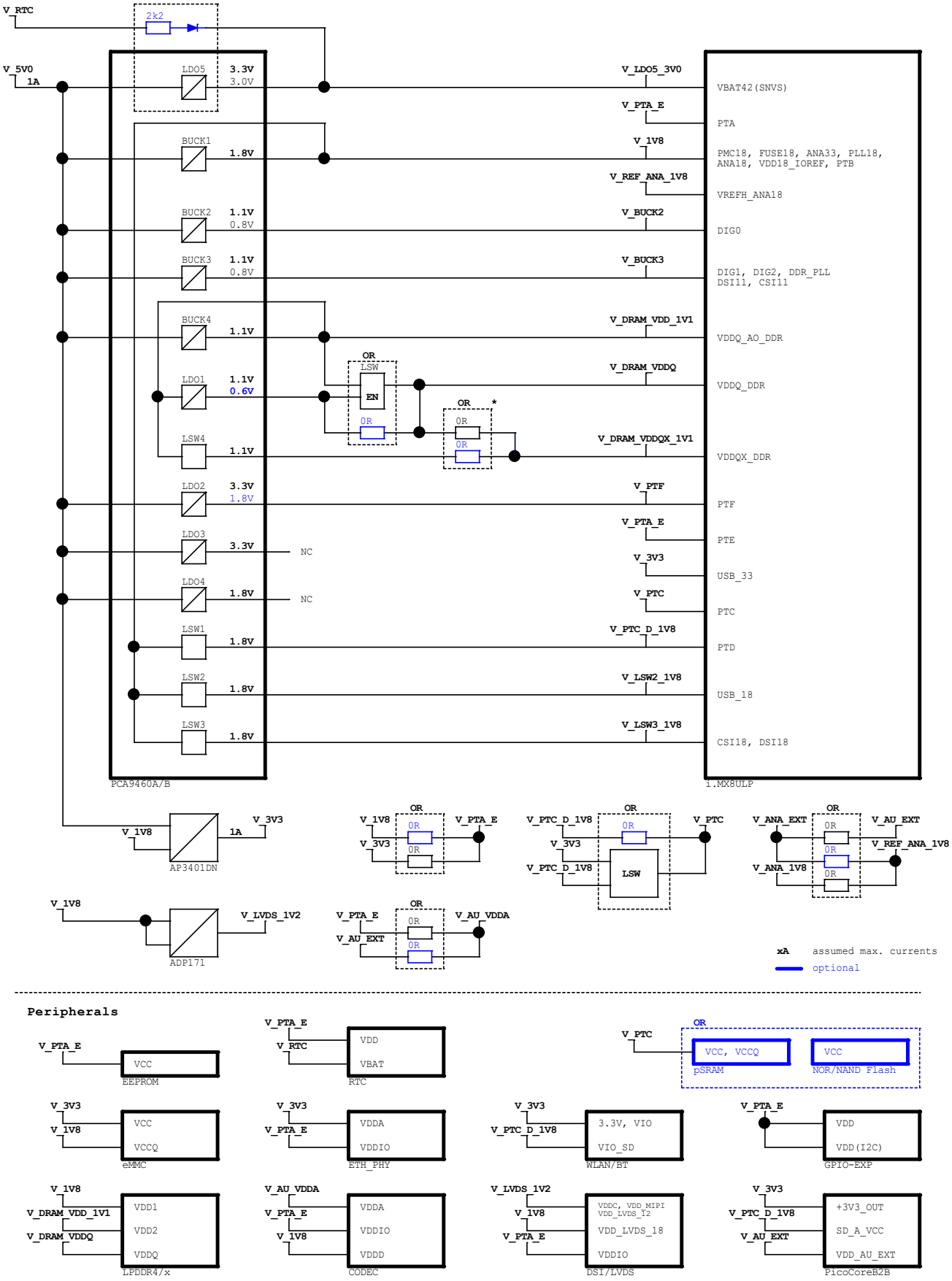


Figure 5: Power (topology)

2.1.4 System Control

The following picture visualizes the system control topology of the module

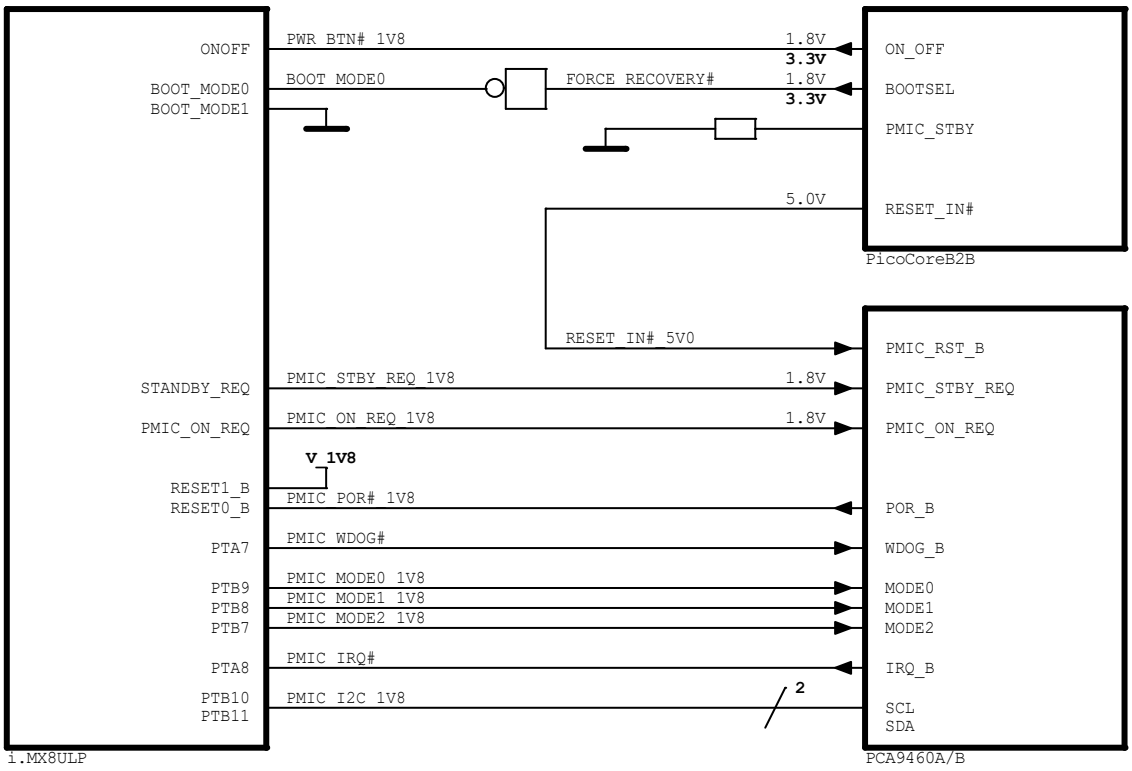


Figure 6: System Control (topology)

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J2	42	RESET_IN#	PCA9460A/B: PMIC_RST_B	I	5.0V	PU 10k, logic LOW resets the module
	44	PMIC_STBY	Not connected			Optional tied to GND
	48	ON_OFF	ONOFF	I	1.8V	PU 10k, behavior depends on the configuration
	50	BOOTSEL[2]	~~BOOT_MODE0~~	I	~~3.3V (1.8V)~~[1]	~~PU 10k~~ ~~HIGH/FLOAT: boots from internal fuses~~ ~~LOW: USB Serial Download mode~~

Table 4: System Control (pin description)

[1] V_PTA_E (PTA & PTE domain voltage).

[2] **IMPORTANT NOTE:** BOOTSEL-pin is non-functional in Rev.1.30.

2.2 Interfaces

2.2.1 JTAG

JTAG is for debug only. The following table shows the intended use of the JTAG[1,2] pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J2	93	JTAG_TCK	PTA23	I	1.8 V	
	95	JTAG_TMS	PTA20	I	1.8 V	
	97	JTAG_TDI	PTA22	I	1.8 V	
	99	JTAG_TDO	PTA21	O	1.8 V	

Table 5: JTAG (pin description)

[1] Do not put the JTAG of the module in a JTAG chain, because different power sequence and power level could kill the CPU.

[2] In addition to JTAG, one will have access to the Cortex®-A35 and Cortex®-M33 cores via serial console. See chapter UART.

2.2.2 UART

The module provides four Universal Asynchronous Receiver Transmitter (UART) ports. The following table shows the use of the UART related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	18	UART_A_RX	PTE11	I	3.3V (1.8V)[1]	Cortex®-A35 debug (APD)
	20	UART_A_TX	PTE10	O	3.3V (1.8V)[1]	Cortex®-A35 debug (APD)
	14	UART_A_RTS	PTE9	O	3.3V (1.8V)[1]	
	16	UART_A_CTS	PTE8	I	3.3V (1.8V)[1]	
	26	UART_B_RX[2]	PTA3	I	3.3V (1.8V)[1]	
	26	UART_B_TX[2]	PTA2	O	3.3V (1.8V)[1]	
	22	UART_B_RTS[2]	PTA17	O	3.3V (1.8V)[1]	
	24	UART_B_CTS[2]	PTA16	I	3.3V (1.8V)[1]	
	30	UART_C_RX	PTE7	I	3.3V (1.8V)[1]	
	32	UART_C_TX	PTE6	O	3.3V (1.8V)[1]	
	34	UART_D_RX	PTA11	O	3.3V (1.8V)[1]	Cortex®-M33 debug (RTD)
	36	UART_D_TX	PTA10	I	3.3V (1.8V)[1]	Cortex®-M33 debug (RTD)

Table 6: UART (pin description)

[1] V_PTA_E (PTA & PTE domain voltage).

[2] Not available when Bluetooth is in use.

2.2.3 Ethernet

Depending on the mounting, the module provides either one as Ethernet(ETH) port:

- a Reduced Media-Independent Interface (RMII)
- a 100BASE-TX Media Dependent Interface (MDI)[1]

The following table shows the use of the ETH related pins on the module.

[1] Used ethernet PHY: Microchip, KSZ80801

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J2	1	ETH_A_D1_P	**KSZ8081:** TXP	O	3.3V	MDI TXP
	3	ETH_A_D1_N	**KSZ8081:** TXN	O	3.3V	MDI TXN
	5	ETH_A_D2_P	**KSZ8081:** RXP	I	3.3V	MDI RXP
	7	ETH_A_D2_N	**KSZ8081:** RXN	I	3.3V	MDI RXN
	17	ETH_A_LED	**KSZ8081:** LED0	O	3.3V	Driven over MOSFET *No Link:* HIGH[1] *Link:* LOW[1] *Act:* TOGGLE

Table 7: ETH MDI (pin description)

[1] Can be inverted as a mounting option.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J2	1	ETH_A_D1_P	PTE15	O	3.3V (1.8V)[2]	MDC
	3	ETH_A_D1_N	PTE14	O	3.3V (1.8V) [2]	MDIO
	5	ETH_A_D2_P	PTE16	O	3.3V (1.8V) [2]	RMII TX EN
	9	ETH_A_D3_P	PTE23	0	3.3V (1.8V) [2]	RMII TXD0
	11	ETH_A_D3_N	PTE22	0	3.3V (1.8V) [2]	RMII TXD1
	13	ETH_A_D4_P	PTE19	I	3.3V (1.8V) [2]	RMII RX CLK
	23	ETH_B_D1_P	PTE18	I	3.3V (1.8V) [2]	RMII RX DV
	25	ETH_B_D1_N	PTE17	I	3.3V (1.8V) [2]	RMII RX ER

	27	ETH_B_D2_P	PTE21	I	3.3V (1.8V) [2]	RMII RXD1
	29	ETH_B_D2_N	PTE20	I	3.3V (1.8V) [2]	RMII RXD0
	35	ETH_B_D4_P	**GPIO Exp.:** P1_6	I	3.3V (1.8V) [2]	Interrupt
	37	ETH_B_D4_N	**GPIO Exp.:** P1_5	O	3.3V (1.8V) [2]	Reset

Table 8: ETH RMII (pin description)

[2] V_PTA_E (PTA & PTE domain voltage).

2.2.4 GPIO

Besides the PWM and ADC signals, the module provides up to 22 additional, free programmable General Purpose Input/Output (GPIO) signals[1,2]. The i.MX8ULP processor contains Standard-GPIOs (STGPIO, domains: PTC, PTD) and Fail-Safe-GPIOs (FSGPIO, domains: PTA, PTB, PTE, PTF). The following table shows the use of the GPIO related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	1	I2C_B_IRQ#	PTA18	I/O	3.3V (1.8V) [5]	Suggested interrupt pin for I2C
	9	DISP_BL_EN	GPIO Exp.: P1_0	I/O	3.3V (1.8V) [1]	Suggested for display control, see 2.2.17
	11	DISP_BL_PWM	PTF29	I/O	3.3V[2]	
	13	DISP_VDD_EN	GPIO Exp.: P1_1	I/O	3.3V (1.8V) [1]	
	74	CSI_CLK_P[6]	PTF28	I/O	3.3V[3]	
	76	CSI_CLK_N[6]	PTF30	I/O	3.3V[3]	
	80	CSI_D0_P[6]	PTF31	I/O	3.3V[3]	
	82	CSI_D0_N[6,7]	PTC19	I/O	3.3V (1.8V) [4]	
	86	CSI_D1_P[6,7]	PTE2	I/O	3.3V (1.8V) [5]	
	88	CSI_D1_N[6]	PTC0	I/O	3.3V (1.8V) [4]	
J2	15	ETH_A_D4_N	**GPIO Exp.:** P0_5	I/O	3.3V (1.8V) [5]	
	21	ETH_B_LED	**GPIO Exp.:** P0_6	I/O	3.3V (1.8V) [5]	
	31	ETH_B_D3_P	PTC11	I/O	3.3V (1.8V) [4]	Clock Out
	33	ETH_B_D3_N	PTA8	I/O	3.3V (1.8V) [5]	Wake Up Unit (WUU)
	54	SD_A_VSEL[7]	PTC20	O	3.3V (1.8V) [4]	
	60	SD_A_CD#	PTC23	I	3.3V (1.8V) [4]	Clock out
	67	GPIO_J2_67	PTC5	I/O	3.3V (1.8V) [4]	
	69	GPIO_J2_69	PTC6	I/O	3.3V (1.8V) [4]	
	77	GPIO_J2_77	PTB14	I/O	1.8V	
	79	GPIO_J2_79	PTB15	I/O	1.8V	
	98	SD_B_D2	PTB12	I/O	1.8V	Suggested CSI MCLK (Master Clock)
	100	SD_B_D3	PTB13	I/O	1.8V	

Table 9: GPIO (pin description)

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the GPIO contacts, it must be ensured that no voltage is applied on any GPIO pin on a non-powered module.

[3] V_PTF (PTF domain voltage) can be changed in steps of 50 mV (programmable via I²C).

[4] V_PTC (PTC domain voltage).

[5] V_PTA_E (PTA & PTE domain voltage).

[6] Not available when MIPI CSI is used.

[7] Not available when psRAM / OctalSPI Flash is mounted.

2.2.5 SDIO

The module provides one Secure Digital Input Output (SDIO) interface[1]. The following table shows the use of the SDIO related pins on the module.

Note: For specification and licensing please refer to the website of the SD Association http://www.sdcard.org.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
	56	SD_A_RST#	PTD13	O	1.8V[2]	Reset, low active
	62	SD_A_CMD	PTD23	I/O	1.8V[2]	PU 10k
	64	SD_A_CLK	PTD22	O	1.8V[2]	
	66	SD_A_D0	PTD21	I/O	1.8V[2]	PU 10k
	68	SD_A_D1	PTD20	I/O	1.8V[2]	
	70	SD_A_D2	PTD19	I/O	1.8V[2]	
	72	SD_A_D3	PTD18	I/O	1.8V[2]	
	74	SD_A_D4	PTD17	I/O	1.8V[2]	2nd: Write Protect[3], PU: CPU internal
	76	SD_A_D5	PTD16	I/O	1.8V[2]	2nd: Card Detect, low active[3], PU: CPU internal
	78	SD_A_D6	PTD15	I/O	1.8V[2]	2nd: Voltage Select[3]
	80	SD_A_D7	PTD14	I/O	1.8V[2]	

Table 10: SDIO (pin description)

[1] Not available when Wi-Fi module is mounted.

[2] When SDIO_A is intended to be used with SD/MMC cards, a suitable level-translator is required on the carrier.

[3] Required when using an SD Card with 4 bit SDIO.

2.2.6 PWM

The module provides up to 4 free programmable Pulse Width Modulation (PWM) signals[1,2]. The following table shows the use of the PWM related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	11	BL_PWM	PTF29	O	3.3V[3]	Backlight brightness control
J2	58	SD_A_WP[4]	PTC12	O	3.3V (1.8V)[5]	
	63	PWM	PTC1	O	3.3V (1.8V)	
	65	GPIO_J2_65	PTC2	O	3.3V (1.8V)	

Table 11: PWM (pin description)

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the PWM contacts it must be ensured that no voltage is applied on any PWM pin on a non-powered module.

[3] V_PTF (PTF domain voltage) can be changed in steps of 50 mV (programmable via I^2C).

[4] Not available when psRAM / OctalSPI Flash is mounted.

[5] V_PTC (PTC domain voltage).

2.2.7 Analog Signals

The i.MX8ULP processor contains two dedicated 12-bit Digital-Analog-Converter (DAC) and seven 12-bit Analog-Digital-Converter (ADC). The ADC signals can be used in differential or single-end mode. In differential mode the result of the ADC is (CHnA – CHnB) or (CHnB – CHnA). The following table shows the use of the analog related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J2	73	GPIO_J2_73	DAC0_OUT	O	1.8V[1]	
	75	GPIO_J2_75	DAC1_OUT	O	1.8V[1]	

Table 12: DAC (pin description)

[1] As a mounting option, the analog reference voltage can be selected from internal or external source. See chapter 2.1.1.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J2	84	SD_B_RST#	PTB0	I	1.8V[1]	ADC0 CH0A
	86	SD_B_WP	PTB1	I	1.8V[1]	ADC0 CH0B
	88	SD_B_CD#	PTB2	I	1.8V[1]	ADC0 CH1A

	90	SD_B_CMD	PTB3	I	1.8V[1]	ADC0 CH1B
	92	SD_B_CLK	PTB4	I	1.8V[1]	ADC0 CH2A
	94	SD_B_D0	PTB5	I	1.8V[1]	ADC0 CH2B
	96	SD_B_D1	PTB6	I	1.8V[1]	ADC0_CH3A

Table 13: ADC (pin description)

[1] As a mounting option, the analog reference voltage can be selected from internal or external source. See chapter 2.1.1.

2.2.8 SPI

The module provides three Serial Peripheral Interface (SPI) ports. The following table shows the use of the SPI related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	64	SPI_A_CS0#[1]	PTC17	O	3.3V (1.8V)[2]	
	66	SPI_A_MISO[1]	PTC21	I	3.3V (1.8V)[2]	
	68	SPI_A_MOSI[1]	PTC22	O	3.3V (1.8V)[2]	
	70	SPI_A_SCK[1]	PTC18	O	3.3V (1.8V)[2]	
	58	SPI_B_CS0#	PTA19	O	3.3V (1.8V)[3]	
	60	SPI_B_MISO	PTA4	I	3.3V (1.8V)[3]	
	62	SPI_B_MOSI	PTA5	O	3.3V (1.8V)[3]	
	64	SPI_B_SCK	PTA6	O	3.3V (1.8V)[3]	
J2	83	SPI_C_CS0#[1]	PTC16	O	3.3V (1.8V)[2]	
	85	SPI_C_MISO[1]	PTC13	I	3.3V (1.8V)[2]	
	87	SPI_C_MOSI[1]	PTC14	O	3.3V (1.8V)[2]	
	89	SPI_C_SCK[1]	PTC15	O	3.3V (1.8V)[2]	

Table 14: SPI (pin description)

[1] Not available when pSRAM / OctalSPI Flash is mounted.

[2] V_PTC (PTC domain voltage).

[3] V_PTA_E (PTA & PTE domain voltage).

2.2.9 OctalSPI

The module provides one Octal Serial Peripheral Interface (OctalSPI) port[1]. The following table shows the use of the Octal-SPI related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	64	SPI_A_CS0#	PTC17		3.3V (1.8V)[2]	OctalSPI CS#
	70	SPI_A_SCK	PTC18		3.3V (1.8V)[2]	OctalSPI CLK
	68	SPI_A_MOSI	PTC22		3.3V (1.8V)[2]	OctalSPI DQ0
	66	SPI_A_MISO	PTC21		3.3V (1.8V)[2]	OctalSPI DQ1
J2	54	SD_A_VSEL	PTC20		3.3V (1.8V)[2]	OctalSPI DQ2
	82	CSI_D0_N	PTC19		3.3V (1.8V)[2]	OctalSPI DQ3
	83	SPI_C_CS0#	PTC16		3.3V (1.8V)[2]	OctalSPI DQ4
	89	SPI_C_SCK	PTC15		3.3V (1.8V)[2]	OctalSPI DQ5
	87	SPI_C_MOSI	PTC14		3.3V (1.8V)[2]	OctalSPI DQ6
	85	SPI_C_MISO	PTC13		3.3V (1.8V)[2]	OctalSPI DQ7
	58	SD_A_WP	PTC12		3.3V (1.8V)[2]	OctalSPI DQS

Table 15: OctalSPI (pin description)

[1] Not available when pSRAM / OctalSPI Flash is mounted.

[2] V_PTC (PTC domain voltage).

2.2.10 Audio

For Audio (AU) the module provides either:

- an audio codec[1]
- an I2S interface.

[1] Used codec: NXP, SGTL5000

The following table shows the use of the Audio related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J2	12	AU_LIN_L	PTC10	I/O	3.3V (1.8V)[1]	I2S MCLK[2]
	8	AU_LOUT_R	PTC9	I/O	3.3V (1.8V)[1]	I2S LRCLK[2]
	6	AU_LOUT_L	PTC8	O	3.3V (1.8V)[1]	I2S BITCLK
	20	AU_HP_R	PTC4	I	3.3V (1.8V)[1]	I2S DATA IN
	18	AU_HP_L	PTC7	O	3.3V (1.8V)[1]	I2S DATA OUT

Table 16: AU I2S (pin description)

[1] V_PTC (PTC domain voltage).

[2] Output, if module acts in Master Mode. Input, if module acts in Slave Mode.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J2	6	AU_LOUT_L	**SGTL5000:** LOUT	O	1.5V / 2.6V[1]	Line out left
	8	AU_LOUT_R	**SGTL5000:** ROUT	O	1.5V / 3.1V[1]	Line out left
	10	AU_MIC	**SGTL5000:** MICIN	I	1.6V / 2.8V[1]	Microphone
	12	AU_LIN_L	**SGTL5000:** LLINEIN	I	1.6V / 2.8V[1]	Line in left
	14	AU_LIN_R	**SGTL5000:** RLINRIN	I	1.6V / 2.8V[1]	Line in right
	18	AU_HP_L	**SGTL5000:** LHPOUT	O	1.5V / 2.6V[1]	Headphone left
	20	AU_HP_R	**SGTL5000:** RHPOUT	O	1.5V / 2.6V[1]	Headphone right

Table 17: AU Analog (pin description)

[1] Voltage depends on analog voltage supply V_AU_VDDA (1.8V / 3.3V). Depending on mounting options, V_AU_VDD is either V_PTA_E or V_AU_EXT

2.2.11 CAN

The module provides one Controller Area Network Interface (CAN). The following table shows the use of the CAN related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	10	CAN_A_RX	PTA13	I	3.3V (1.8V)[1]	
	12	CAN_A_TX	PTA12	O	3.3V (1.8V)[1]	

Table 18: CAN (pin description)

[1] V_PTA_E (PTA & PTE domain voltage).

2.2.12 USB

The module provides two Universal Serial Busses (USB)[1], including controllers and PHYs. The following table shows the use of the USB related pins on the module.

[1] One is Host only, one is an On the Go (OTG) port

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J2	41	USB_HOST_VBUS	USB1_VBUS_DETECT	I	5.0V	USB VBUS detection port A[1]
	45	USB_HOST_D_N	USB1_DN	I/O	USB	
	43	USB_HOST_D_P	USB1_DP	I/O	USB	
	47	USB_HOST_PWR	**GPIO Exp.:** P1_3	O	3.3V (1.8V)[2]	
	51	USB_OTG_VBUS	USB0_VBUS_DETECT	I	5.0V	USB VBUS detection port B[1]
	53	USB_OTG_PWR	**GPIO Exp.:** P1_4	O	3.3V (1.8V)[2]	
	55	USB_OTG_ID	PTD12	I	3.3V (1.8V)[2]	PU 10k
	59	USB_OTG_D_N	USB0_DN	I/O	USB	
	57	USB_OTG_D_P	USB0_DP	I/O	USB	

Table 19: USB (pin description)

[1] Must always be connected to the respective USB VBUS rail.

[2] V_PTA_E (PTA & PTE domain voltage).

2.2.13 I2C

The module provides five Inter-Integrated Circuit (I2C) interfaces which are connected to the following components.

I2C	Connected To	Address	Comments
PMIC	PMIC	0x32	Power Management IC on the module, Type: NXP, PCA9460A
INT[1,2]	Audio Codec	0x0A	Audio Codec, Type: NXP, SGTL5000
	RTC	0x51	RTC on the module (accessible from carrier), Type: NXP, PCF85263ATL
	GPIO Exp.	0x20	16bit GPIO Expander, Type: NXP, PCAL6416A
	DSI/LVDS	0x0F	DSI to LVDS converter, Type: Toshiba, TC358775XBG
A	EEPROM	0x50	EEPROM on the module (accessible from carrier), Type: ON, N24S64B
	Connector J1	-	general I2C on carrier
B	Connector J1	-	general I2C on carrier
C	Connector J1	-	general I2C on carrier
D	Connector J1	-	general I2C on carrier

Table 20: I2C (usage)

[1] For internal use only.

[2] Connected to PTA14 / PTA15 (SCL / SDA)

The following table shows the use of the I2C related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	4	I2C_A_SCL	PTE12	O	3.3V (1.8V)[1]	PU 2.2 kΩ
	6	I2C_A_SDA	PTE13	I/O	3.3V (1.8V)[1]	PU 2.2 kΩ
	3	I2C_B_SCL	PTA0	O	3.3V (1.8V)[1]	PU 2.2 kΩ
	5	I2C_B_SDA	PTA1	I/O	3.3V (1.8V)[1]	PU 2.2 kΩ
	1	I2C_B_IRQ#	PTA18	I/O	3.3V (1.8V)[1]	PU: CPU internal., Interrupt pin for I2C
	40	I2C_C_SCL	PTE0	O	3.3V (1.8V)[1]	PU 2.2 kΩ
	42	I2C_C_SDA	PTE1	I/O	3.3V (1.8V)[1]	PU 2.2 kΩ
	48	I2C_D_SCL	PTE4	O	3.3V (1.8V)[1]	PU 2.2 kΩ
	50	I2C_D_SDA	PTE5	I/O	3.3V (1.8V)[1]	PU 2.2 kΩ

Table 21: I2C (pin description)

[1] V_PTA_E (PTA & PTE domain voltage).

2.2.14 MIPI CSI

The module provides one 2 lane Camera Serial Interface (CSI)[1], defined by the Mobile Industry Processor Interface Alliance (MIPI), compliant with MIPI CSI-2 specification v1.1 and MIPI D-PHY specification v1.1. The following table shows the use of the MIPI CSI related pins on the module.

[1] Not available when psRAM / OctalSPI Flash is mounted or used as GPIOs.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	74	CSI_CLK_P	CSI_CLK_P	I	MIPI CSI	Clock
	76	CSI_CLK_N	CSI_CLK_N	I	MIPI CSI	Clock
	80	CSI_D0_P	CSI_DATA0_P	I	MIPI CSI	
	82	CSI_D0_N	CSI_DATA0_N	I	MIPI CSI	
	86	CSI_D1_P	CSI_DATA1_P	I	MIPI CSI	
	88	CSI_D1_N	CSI_DATA1_N	I	MIPI CSI	
J2	98	SD_B_D2	PTB12	O	1.8V	CSI MCLK (Master Clock)

Table 22: CSI (pin description)

2.2.15 Display

As a mounting option, the module provides either one of the following display ports:

- 4 lane Display Serial Interface (DSI), natively from the CPU
- 4 lane Low Voltage Differential Signal (LVDS) display interface, converted[1] from the DSI.
  LVDS is not working on Rev 1.20! It is planned to be fixed in the next revision. The pinout will be kept the same.

The following table shows the use of the DISP related pins on the module.

[1] Used converter type: Toshiba, TC358775XBG

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	17	DISP_CLK_P	DSI_CLK_P	O	DSI	DSI Clock
	19	DISP_CLK_N	DSI_CLK_N	O	DSI	
	23	DISP_D0_P	DSI_DATA0_P	O	DSI	DSI Data 0
	25	DISP_D0_N	DSI_DATA0_N	O	DSI	
	29	DISP_D1_P	DSI_DATA1_P	O	DSI	DSI Data 1
	31	DISP_D1_N	DSI_DATA1_N	O	DSI	
	35	DISP_D2_P	DSI_DATA_P	O	DSI	DSI Data 2
	37	DISP_D2_N	DSI_DATA2_N	O	DSI	
	41	DISP_D3_P	DSI_DATA3_P	O	DSI	DSI Data 2
	43	DISP_D3_N	DSI_DATA3_N	O	DSI	

Table 23: DSI (pin description)

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	17	DISP_CLK_P	TC358775XBG	O	LVDS	LVDS Clock
	19	DISP_CLK_N	TC358775XBG	O	LVDS	
	23	DISP_D0_P	TC358775XBG	O	LVDS	LVDS Data 0
	25	DISP_D0_N	TC358775XBG	O	LVDS	
	29	DISP_D1_P	TC358775XBG	O	LVDS	LVDS Data 1
	31	DISP_D1_N	TC358775XBG	O	LVDS	
	35	DISP_D2_P	TC358775XBG	O	LVDS	LCDS Data 2
	37	DISP_D2_N	TC358775XBG	O	LVDS	
	41	DISP_D3_P	TC358775XBG	O	LVDS	LVDS Data 2
	43	DISP_D3_N	TC358775XBG	O	LVDS	

Table 24: LVDS (pin description)

2.2.16 RGB

The module provides one 24-bit RGB Display Interface. The following table shows the use of the RGB related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	44	GPIO_J1_44	PTF23	O	3.3V[1]	RGB Red 0
	59	DISP_B_D1_P	PTF22	O	3.3V[1]	RGB Red 1
	46	GPIO_J1_46	PTF21	O	3.3V[1]	RGB Red 2
	49	DISP_B_CLK_N	PTF20	O	3.3V[1]	RGB Red 3
	54	GPIO_J1_54	PTF19	O	3.3V[1]	RGB Red 4
	65	DISP_B_D2_P	PTF18	O	3.3V[1]	RGB Red 5
	52	GPIO_J1_52	PTF17	O	3.3V[1]	RGB Red 6
	83	mPCIE_RX_P	PTF16	O	3.3V[1]	RGB Red 7
	85	mPCIE_RX_N	PTF15	O	3.3V[1]	RGB Green 0
	61	DISP_B_D1_N	PTF14	O	3.3V[1]	RGB Green 1
	92	CSI_D2_P	PTF13	O	3.3V[1]	RGB Green 2
	67	DISP_B_D2_N	PTF12	O	3.3V[1]	RGB Green 3
	89	mPCIE_CLK_P	PTF11	O	3.3V[1]	RGB Green 4
	91	mPCIE_CLK_N	PTF10	O	3.3V[1]	RGB Green 5
	98	CSI_D3_P	PTF9	O	3.3V[1]	RGB Green 6
	71	DISP_B_D3_P	PTF8	O	3.3V[1]	RGB Green 7
	100	CSI_D3_N	PTF7	O	3.3V[1]	RGB Blue 0
	73	DISP_B_D3_N	PTF6	O	3.3V[1]	RGB Blue 1
	95	mPCIE_PERST#	PTF5	O	3.3V[1]	RGB Blue 2
	47	DISP_B_CLK _P	PTF4	O	3.3V[1]	RGB Blue 3
	79	mPCIE_TX_N	PTF3	O	3.3V[1]	RGB Blue 4
	94	CSI_D2_N	PTF2	O	3.3V[1]	RGB Blue 5
	77	mPCIE_TX_P	PTF1	O	3.3V[1]	RGB Blue 6
	97	mPCIE_WAKE#	PTF0	O	3.3V[1]	RGB Blue 7
	55	DISP_B_D0_N	PTF24	O	3.3V[1]	RGB Clock
	2	GPIO_J1_2	PTF25	O	3.3V[1]	RGB Vertical Synchronization
	7	GPIO_J1_7	PTF26	O	3.3V[1]	RGB Horizontal Synchronization
	53	DISP_B_D0_P	PTF27	O	3.3V[1]	RGB Data Enable

Table 25: RGB (pin description)

[1] V_PTF (PTF domain voltage) can be changed in steps of 50 mV (programmable via I²C).

2.2.17 Display Control

To control a display, there are several suggested GPIOs. The following table shows the related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	9	DISP_BL_EN	GPIO Exp.: P1_0	I/O	3.3V (1.8V) [1]	Backlight enable
	11	DISP_BL_PWM	PTF29	I/O	3.3V[2]	Backlight brightness control
	13	DISP_VDD_EN	GPIO Exp.: P1_1	I/O	3.3V (1.8V) [1]	Display enable

Table 26: Display Control (pin description)

[1] V_PTA_E (PTA & PTE domain voltage).

[2] V_PTF (PTF domain voltage) can be changed in steps of 50 mV (programmable via I²C).

2.2.18 Requirements for Unused Interfaces

The following table shows the use of the required connections for unused interfaces.

Ref.	Pin	Contact Name	Internal Pad	Requirement
J2	41	USB_HOST_VBUS	USB1_VBUS_DETECT	10kΩ to Ground
	51	USB_OTG_VBUS	USB0_VBUS_DETECT	10kΩ to Ground

Table 27: Unused Interfaces (pin description)

2.3 Internal Peripherals on the Module

2.3.1 LPDDR4 / LPDDR4x

The module contains one 32-bit LPDDR4/x[1] SDRAM which operates with up to 1056 MT/s.

[1] optional

2.3.2 eMMC

The module contains one Embedded MultiMedia Card (eMMC) Flash memory. eMMCs have limited erasing cycles, and the data retention depends on the temperature. It is important to know that high temperatures above 50°C significantly impact the data retention of the eMMC[1], independently whether the device is powered or not.

[1] Please contact us for more information about data retention on eMMCs in high temperature environments.

2.3.3 pSRAM / OctalSPI Flash

The module offers the possibility of mounting a pSRAM or OctalSPI Flash as an additional memory[1]. The following picture visualizes the pSRAM / OctaclSPI Flash options.

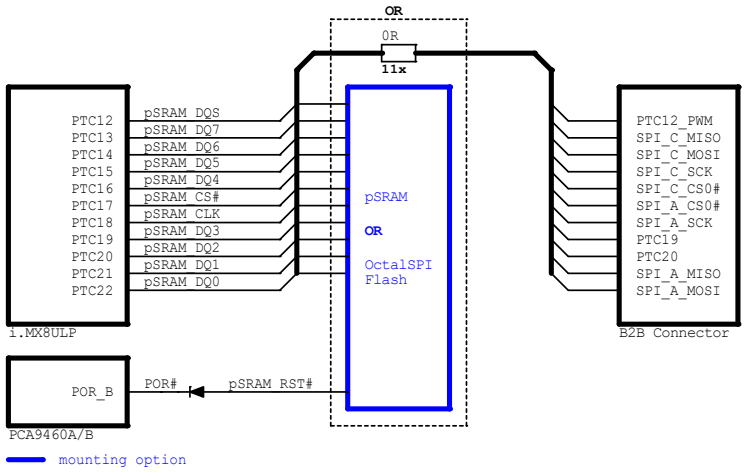


Figure 7: pSRAM / OctalSPI Flash (mounting option)

[1] SPI_A, some GPIOs & PWM_5 are not available at the contact grid, when this option is used.

2.3.4 RTC

The module contains a Real Time Clock (RTC, Type: PCF85263ATL)[1] which is connected to I2C_INT (address: 0x51). The time can be maintained by applying a suitable voltage to V_RTC even if the module itself is not powered.

[1] Cause the accuracy is limited by the crystal, the RTC could drift some seconds per day.

Optionally, the discrete RTC can be replaced by the internal RTC of the i.MX8ULP. With this option, the security batt domain of the i.MX8ULP remains supplied, even if the rest of the module itself is not supplied. The disadvantage is a significant higher battery current. The following picture visualizes the RTC options.

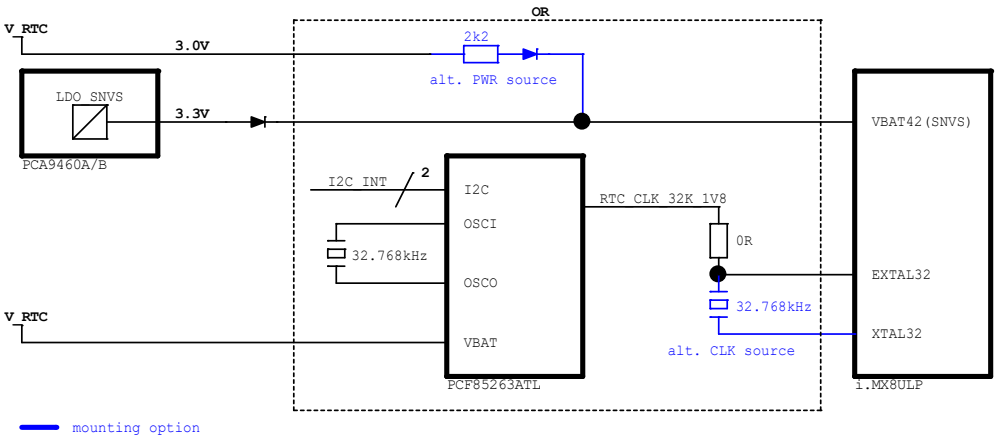


Figure 8: RTC (mounting options)

2.3.5 EEPROM

The module contains a 64Kb Electrically Erasable Programmable Read-Only Memory (EEPROM) (Type: N24S64B) which is connected to I2C_A (address: 0x50)

2.3.6 Wi-Fi & Bluetooth

This module contains a certified high-performance Wi-Fi and Bluetooth module[1] with:

- IEEE802.11 a/b/g/n/ac
- Bluetooth 2.1 and 3.0 + Enhanced Data Rate (EDR) +BT 5.3[2]

It is based on the NXP 88W8997 chip with various certifications[3] (e.g. RED, FCC, Giteki, etc.).

[1] Wi-Fi/BT module type: Azure Wave, CM276NF

[2] UART B is not available when BT is in use.

[3] Please contact support@fs-net.de for additional information about the process of certification.

3 Characteristics

3.1 Absolute Maximum Ratings[1]

Parameter	Description	Min	Max	Unit
V_{5V0}	main power input voltage at the V_5V_IN pins	-0.50	6.00	V
V_{RTC}	RTC battery input voltage at the RTC_PWR pin	-0.30	4.50	V
V_{IO}	general I/O voltage (V_{DD} … nominal I/O voltage)	-0.15	V_{DD} + 0.15	V
V_{AU_EXT}	External audio (analog signal) reference input	0.00	3.60 (1.98[2])	V
USB VBUS	PHY detection signal of USB port supply voltage on the carrier	-0.30	5.60	V

Table 28: Absolute Maximum Ratings

[1] Stresses beyond the listed values may affect reliability or cause permanent damage to the module.

[2] Absolute max. value when used as analog signal reference input.

3.2 Recommended Operating Conditions

Parameter	Description	Condition	Min	Typ	Max	Unit
General						
V_{5V0}	main power input		4.50	5.00	5.50	V
I_{5V0}					1.00	A
V_{RTC}	RTC battery input	contact: **J2.36** V_{RTC} = 3.0 V	2.50	3.00	4.00	V
I_{RTC}				0.35	100	µA
USB VBUS	PHY detection of USB VBUS	contact: **J2.41, J2.51**		5.00		V
V_{3V3_OUT}	supply output (general I/O reference)	contact: **J2.40**		3.30		V
I_{3V3_OUT}					250	mA
$V_{SD\_A\_VCC}$	supply output (SDIO_A I/O reference)	contact: **J2.52**		1.80		V
$I_{SD\_A\_VCC}$					100	mA
Standard GPIO (STGPIO)						
V_{IH}	STGPIO I/O high-level input voltage	PTC: V_{DD} = 1.8 V / 3.3 V	0.7 · V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	STGPIO I/O low-level I/O input voltage		0		0.3 · V_{DD}	V
V_{OH}	STGPIO I/O high-level output voltage	PTD, PTB: V_{DD} = 1.8 V	0.8 · V_{DD}		V_{DD}	V
V_{OL}	STGPIO I/O low-level I/O output voltage				0.125 · V_{DD}	V
Fail-Safe GPIO (FSGPIO)						
V_{IH}	FSGPIO I/O high-level input voltage	PTA, PTE, PTF: V_{DD} = 1.8 V / 3.3 V	1.35	V_{DD}	V_{DD}	V
V_{IL}	FSGPIO I/O low-level I/O input voltage		0		0.54	V
V_{OH}	FSGPIO I/O high-level output voltage		V_{DD} – 0.5		V_{DD}	V
V_{OL}	FSGPIO I/O low-level I/O output voltage				0.5	V
12-bit DAC						
C_L	output load capacitance			50	100	pF
I_L	output load current				±1	mA
$VDAC_{OUTL}$	DAC low level output voltage	R_L = 18 kΩ, C_L = 50 pF	0		0.15[3]	V
$VDAC_{OUTH}$	DAC high level output voltage		1.65[1]		1.80	V
12-bit ADC						
C_L	input load capacitance			4.50		pF
R_{IN}	input resistance			500		Ω

Temperatures						
$T_{OPERATE}$	operating temperature range[2]	C TEMP grade	0		70	°C
		I TEMP grade	-25		85	°C
		XI TEMP grade	-40		85	°C
$T_{STORAGE}$	storage temperature range		-40		85	°C
$t_{STORAGE}$	storage time	no environmental control		6	months	
		T_{AMB} = 25 °C ± 5 °C humidity max. 60 %		12	months	

Table 29: Recommended Operating Conditions

[1] It is recommended to operate the DAC in the output voltage range between 0.15 V … 1.65 V.

[2] An external cooling solution may be required to cover the entire range.

4 Packaging & Labels

4.1 ESD

All F&S electrostatic discharge sensitive (ESDS) products are marked and will be shipped in ESD protective packaging.

4.2 Serial Number

All shipped F&S products are labeled with a matrix code sticker that includes the serial number. For product information visit www.fsembedded.com/en/support/serial-number-info-and-rma/.

5 Appendix

5.1 Second source rules

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5.2 RoHS and REACH statement

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