Hardware Documentation

FS 93 OSM-SF

for HW Revision 1.10

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Elektronik Systeme

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About This Document

This document describes how to use the FS 93 OSM-SF (further named as module) with mechanical and electrical information. The latest version of this document can be found at: www.fsembedded.com/en/osm.

ESD Requirements

All F&S hardware products are electrostatic discharge (ESD) sensitive. All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD sensitive material in ESD unsafe environments. Negligent handling will harm the product and warranty claims become void.

Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

History

Version/Date	Platform	Added (A) Removed (R) Modified (M)	Chapter	Description	Author
001/10.2023	All		-	Initial Version	HF
002/01.2024	All	A	2	Added Heat spreader	TM
003/02.2024	All	M	3.1, 4.10	Correct AB7 and AB8	MW
004/04.2024	All	M	2.1, 2.1.2	information regarding edge overhang added, mechanical dimensions changed	UK, TM
005/01.2025	All	M	9	Changed operating temperature from -20°C to -25°C	HF
006/04.2025	-	A, M, R	All	New design template, major adaptions	UK

Table of Content

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1 Overview

1.1 Additional Documentation

The “OSM Implementation Guide” contains information which are the same for all F&S OSM products, e.g. the

- mechanical description,
- general OSM contact grid signal description,
- handling information.

The latest version can be downloaded from www.fsembedded.com/en/osm.

1.2 General Parameter

Parameter	Description
Dimensions (L x W x H)	(30.0 x 30.0 x 2.0) mm
Weight	≈ 5 g
Pin Count	332 (202 used)

Table 1: General Parameter

1.3 Block Diagram

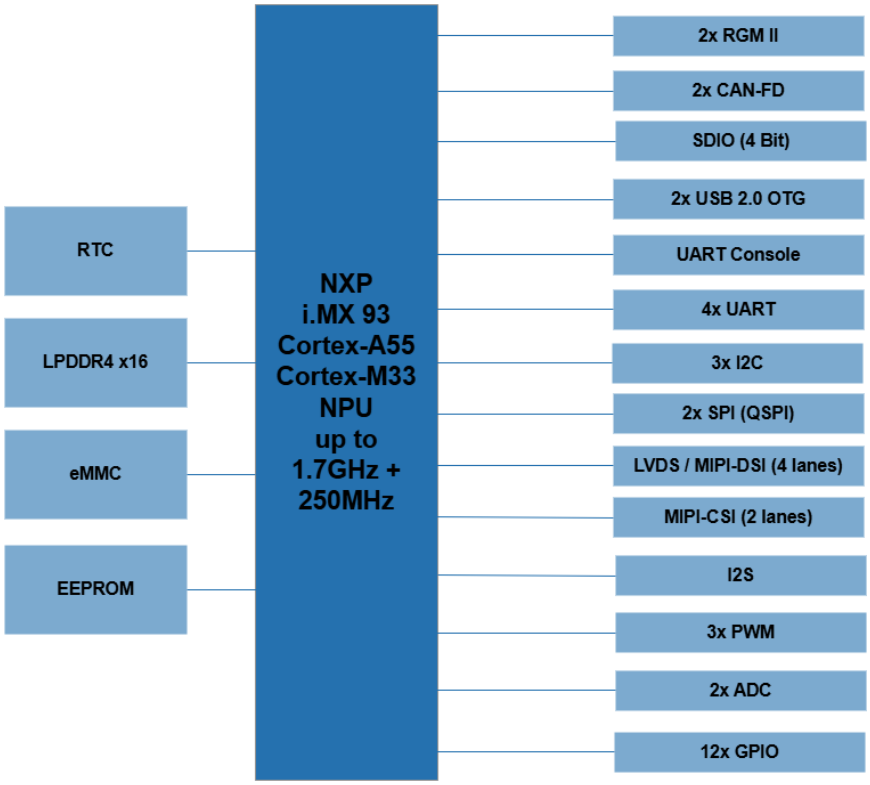

Figure 1: Block Diagram

Note: This diagram shows the maximum available features. The availability depends on the configuration.

1.4 Design Data

To ease the implementation, F&S provides the “OSM Carrier Board Design Library” which contains

- a schematic symbol (Altium & Cadence) including module-specific implementation information,
- the footprint (Altium & Cadence, baseboard side),
- a 3D model.

The latest version can be downloaded from www.fsembedded.com/en/osm.

2 Detailed Description

To increase clarity, the GND[1] pins and all pins which are not connected on the module are not listed in the following sections.

[1] All GND pins are connected on the module. F&S highly recommends to connect all of them on the carrier.

2.1 Power and Management

2.1.1 Power Supply

The following table shows the intended use of the power (PWR) pins on the module.

Contact #	Contact Name	I/O	Voltage	Comments
M19	VCC_2_TEST	PO	1.8 V	1.8 V intended for testing purposes max. current: 50 mA
Y20	VCC_4_TEST	PO	3.3 V	3.3 V intended to supply carrier peripherals max. current: 200 mA
Y8, Y9, Y10, Y11, Y17,	VCC_IN_5V	P	5.0 V	main power supply input
U18	VCC_OUT_IO	PO	1.8 V	general I/O reference voltage max. current: 100 mA
M17	ETH_IOPWR	PO	1.8 V	Ethernet I/O reference voltage max. current: 100 mA
C20	SDIO_A_IOPWR	PO	1.8 V 3.3 V	SDIO_A I/O reference voltage (switchable) max. current: 100 mA
W17	RTC_PWR	P	3.0 V	RTC supply input[1]

Table 2: PWR (pin description)

[1] RTC_PWR may be sourced from a Carrier based Li-cell or Super Cap.

2.1.2 System Control

The following picture visualizes the system control (CTRL) topology of the module.

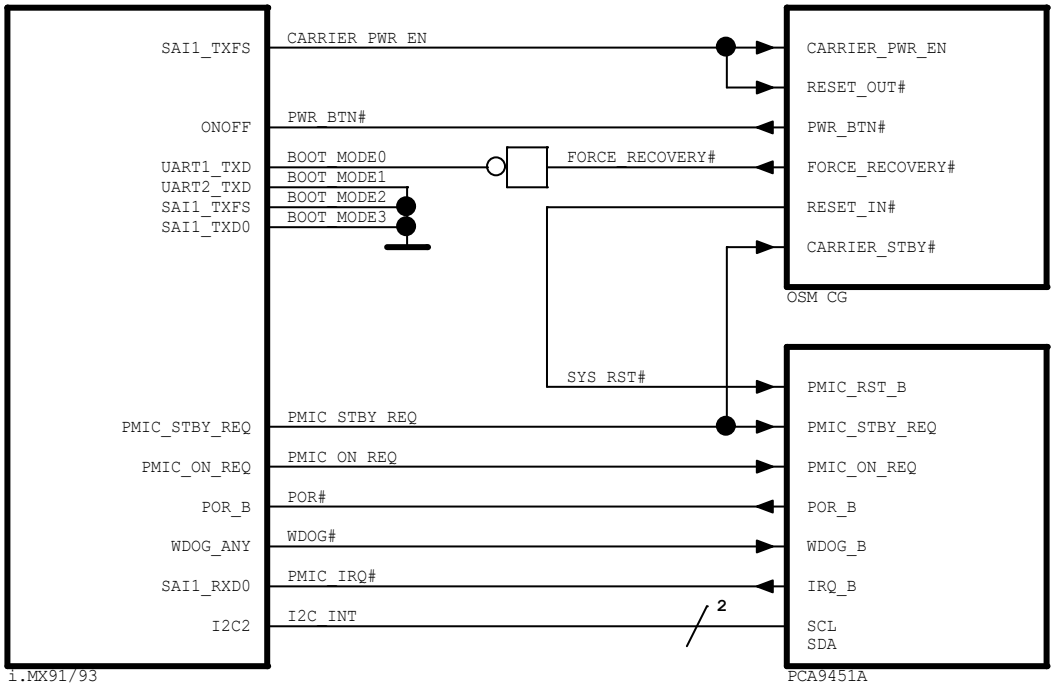

Figure 2: System Control (topology)

The following table shows the intended use of the CTRL pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
V17	CARRIER_PWR_EN	SAI1_TXFS	O	1.8 V	PD 10k, dual function: BOOT_MODE2[2] HIGH active, intended to enable the power for peripherals on carrier
Y13	CARRIER_STBY#	PMIC_STBY_REQ	O	1.8 V	HIGH[3] active, indicates that module is in standby power state
U17	RESET_IN#	**PCA9451A:** PMIC_RST_B	I	1.8 V	PU 10k, logic LOW resets the module
Y14	RESET_OUT#	SAI1_TXFS	O	1.8 V	connected to CARRIER_PWR_EN
AA9	PWR_BTN#[1]	ONOFF	I	1.8 V	PU 10k, behavior depends on the configuration
T17	FORCE_RECOVERY#	UART1_TXD	I	1.8 V	PU 10k HIGH/FLOAT: module boots from internal fuses LOW: module is in USB Serial Download mode

Table 3: System Control (pin description)

[1] PWR_BTN# is debounced inside of the CPU.

[2] The i.MX93 pad is part of the BOOT_CFG. Make sure not to overrule the intended configuration during the startup.

[3] **Please note:** Inverted logic with respect to the definition in the OSM standard.

2.2 Interfaces

2.2.1 MISC

None of the “RESERVED”, “Vendor Defined” & “COM_AREA” pins are connected on the module.

2.2.2 JTAG

JTAG is for debug only. The following table shows the intended use of the JTAG[1,2] pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
N17	JTAG_TCK(SWCLK)	DAP_TCLK_SWCLK	I	1.8 V	firmly connected to GPIO_A_0[3]
N19	JTAG_TMS(SWDIO)	DAP_TMS_SWDIO	I	1.8 V	firmly connected to GPIO_A_1[3]
P17	JTAG_TDI	DAP_TDI	I	1.8 V	firmly connected to CAN_B_TX[3]
R17	JTAG_TDO(SWO)	DAP_TDO_TRACESWO	O	1.8 V	firmly connected to CAN_B_RX[3]

Table 4: JTAG (pin description)

[1] Do not put the JTAG of the module in a JTAG chain, because different power sequence and power level could kill the CPU.

[2] In addition to JTAG, one will have access to the Cortex®-A55 and Cortex®-M33 cores via serial console. See chapter UART.

[3] Do not use this function together with JTAG at the same time.

2.2.3 UART

The module provides up to five[3] Universal Asynchronous Receiver Transmitter (UART) ports. The following table shows the use of the UART related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
A14	UART_A_RX	UART2_RXD	I	1.8 V	
B13	UART_A_TX	UART2_TXD	O	1.8 V	PD 10k, dual function: BOOT_MODE1[2]
C13	UART_A_RTS	SAI1_TXD0	O	1.8 V	PD 10k, dual function: BOOT_MODE3[2]
C14	UART_A_CTS	SAI1_TXC	I	1.8 V	
D14	UART_B_RX	GPIO_IO01	I	1.8 V	
D13	UART_B_TX	GPIO_IO00	O	1.8 V	
D15	UART_B_RTS	GPIO_IO03	O	1.8 V	
D16	UART_B_CTS	GPIO_IO02	I	1.8 V	
A22	UART_C_RX	GPIO_IO15	I	1.8 V	Cortex®-M33 debug
B23	UART_C_TX	GPIO_IO14	O	1.8 V	Cortex®-M33 debug

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
C22	UART_D_RX	GPIO_IO13		1.8 V	
C23	UART_D_TX	GPIO_IO12		1.8 V	
D22	UART_CON_RX	UART1_RXD	I	1.8 V	Cortex®-A55 debug
D23	UART_CON_TX	UART1_TXD	O	1.8 V	PD 10k + LOGIC[1], dual function: BOOT_MODE0[2] Cortex®-A55 debug

Table 5: UART (pin description)

[1] See the information about FORCE_RECOVERY# in chapter System Control.

[2] The i.MX93 pad is part of the BOOT_CFG. Make sure not to overrule the intended configuration during the startup.

[3] The following picture visualizes a mounting option for UART_C & UART_D.

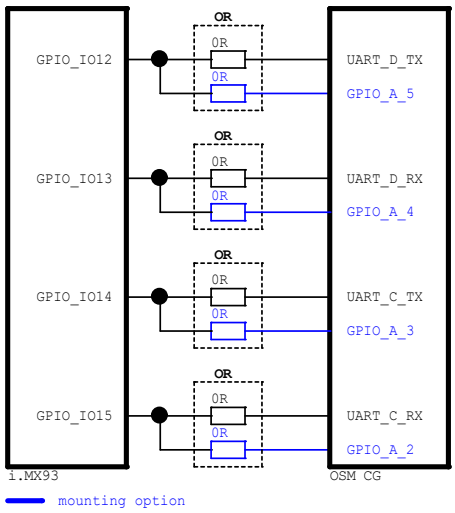

Figure 3: UART (mounting option)

2.2.4 Ethernet

The module provides two Reduced Gigabit Media-Independent Interface (RGMII) Ethernet (ETH) ports. The following table shows the use of the ETH related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
H15	ETH_A_RGMII_TXD0	ENET1_TD0	O	1.8 V	
G15	ETH_A_RGMII_TXD1	ENET1_TD1	O	1.8 V	
H16	ETH_A_RGMII_TXD2	ENET1_TD2	O	1.8 V	
G16	ETH_A_RGMII_TXD3	ENET1_TD3	O	1.8 V	
K16	ETH_A_RGMII_TX_EN(_ER)	ENET1_TX_CTL	O	1.8 V	
J15	ETH_A_RGMII_TX_CLK	ENET1_TXC	O	1.8 V	
K15	ETH_A_RGMII_RXD0	ENET1_RD0	I	1.8 V	
L15	ETH_A_RGMII_RXD1	ENET1_RD1	I	1.8 V	
N15	ETH_A_RGMII_RXD2	ENET1_RD2	I	1.8 V	
P15	ETH_A_RGMII_RXD3	ENET1_RD3	I	1.8 V	
M15	ETH_A_RGMII_RX_DV(_ER)	ENET1_RX_CTL	I	1.8 V	
R15	ETH_A_RGMII_RX_CLK	ENET1_RXC	I	1.8 V	
T15	ETH_A_MDIO	ENET1_MDIO	I/O	1.8 V	shared with ETH_B
T16	ETH_A_MDC	ENET1_MDC	O	1.8 V	shared with ETH_B
G1	ETH_B_RGMII_TXD0	ENET2_TD0	O	1.8 V	
F1	ETH_B_RGMII_TXD1	ENET2_TD1	O	1.8 V	
G2	ETH_B_RGMII_TXD2	ENET2_TD2	O	1.8 V	
F2	ETH_B_RGMII_TXD3	ENET2_TD3	O	1.8 V	

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
J2	ETH_B_RGMII_TX_EN(_ER)	ENET2_TX_CTL	O	1.8 V	
H1	ETH_B_RGMII_TX_CLK	ENET2_TXC	O	1.8 V	
J1	ETH_B_RGMII_RXD0	ENET2_RD0	I	1.8 V	
K1	ETH_B_RGMII_RXD1	ENET2_RD1	I	1.8 V	
M1	ETH_B_RGMII_RXD2	ENET2_RD2	I	1.8 V	
N1	ETH_B_RGMII_RXD3	ENET2_RD3	I	1.8 V	
L1	ETH_B_RGMII_RX_DV(_ER)	ENET2_RX_CTL	I	1.8 V	
P1	ETH_B_RGMII_RX_CLK	ENET2_RXC	I	1.8 V	
C7	ETH_B_MDIO	ENET1_MDIO	I/O	1.8 V	shared with ETH_A
C6	ETH_B_MDC	ENET1_MDC	O	1.8 V	shared with ETH_A

Table 6: ETH (pin description)

2.2.5 GPIO

Besides the PWM signals, the module provides up to 12 additional, free programmable General Purpose Input/Output (GPIO) signals[1,2]. The following table shows the use of the GPIO related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
D17	GPIO_A_0[3]	DAP_TCLK_SWCLK	I/O	1.8 V	firmly connected to JTAG_TCK
E17	GPIO_A_1[3]	DAP_TMS_SWDIO	I/O	1.8 V	firmly connected to JTAG_TMS
F17	GPIO_A_2	GPIO_IO15	I/O	1.8 V	mounting option[4]
G17	GPIO_A_3	GPIO_IO14	I/O	1.8 V	mounting option[4]
H17	GPIO_A_4	GPIO_IO13	I/O	1.8 V	mounting option[4]
J17	GPIO_A_5	GPIO_IO12	I/O	1.8 V	mounting option[4]
K17	GPIO_A_6	ENET2_MDC	I/O	1.8 V	dual function: SPI_A_CS1#
L17	GPIO_A_7	GPIO_IO24	I/O	1.8 V	dual function: SPI_B_CS1#
F3	GPIO_C_4	ENET2_MDIO	I/O	1.8 V	dual function: DISP_VDD_EN
F4	GPIO_C_5	GPIO_IO07	I/O	1.8 V	dual function: DISP_BL_EN
G3	GPIO_C_6	CCM_CLKO2	I/O	1.8 V	dual function: CAM_A_PWR
G4	GPIO_C_7	CCM_CLKO3	I/O	1.8 V	dual function: CAM_A_RST#

Table 7: GPIO (pin description)

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the GPIO contacts, it must be ensured that no voltage is applied on any GPIO pin on a non-powered module.

[3] Do not use this function together with JTAG at the same time.

[4] See the information in chapter UART.

2.2.6 SDIO

The module provides one Secure Digital Input Output (SDIO) interface. The following table shows the use of the SDIO related pins on the module.

Note: For specification and licensing please refer to the website of the SD Association http://www.sdcard.org.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
E20	SDIO_A_CMD	SD2_CMD	I/O	1.8 V[1] 3.3 V[1]	
F21	SDIO_A_CLK	SD2_CLK	O	1.8 V[1] 3.3 V[1]	
G20	SDIO_A_D0	SD2_DATA0	I/O	1.8 V[1] 3.3 V[1]	
G21	SDIO_A_D1	SD2_DATA1	I/O	1.8 V[1] 3.3 V[1]	

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
H20	SDIO_A_D2	SD2_DATA2	I/O	1.8 V[1] 3.3 V[1]	
H21	SDIO_A_D3	SD2_DATA3	I/O	1.8 V[1] 3.3 V[1]	
J21	SDIO_A_CD#	SD2_CD_B	I	1.8 V[1] 3.3 V[1]	PU 10k
D20	SDIO_A_WP	GPIO_IO25	I	1.8 V[1] 3.3 V[1]	
D21	SDIO_A_PWR_EN	SD2_RESET_B	O	1.8 V[1] 3.3 V[1]	

Table 8: SDIO (pin description)

[1] As SDIO_A is intended to be used with SD/MMC cards, the I/O voltage is dynamically switchable between 3.3 V & 1.8 V on the module. The level of SDIO_A_IOPWR depends on the internal signal SDIO_A_VSEL (CPU pad: SD2_VSELECT):

- SDIO_A_VSEL = LOW: SDIO_A_IOPWR = 3.3 V (default)
- SDIO_A_VSEL = HIGH: SDIO_A_IOPWR = 1.8 V

2.2.7 PWM

The module provides up to three free programmable Pulse Width Modulation (PWM) signals[1,2]. The following table shows the use of the PWM related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
E18	PWM_0	GPIO_IO06	O	1.8 V	dual function: DISP_BL_PWM
F18	PWM_1	GPIO_IO04	O	1.8 V	
G18	PWM_2	GPIO_IO05	O	1.8 V	

Table 9: PWM (pin description)

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the PWM contacts it must be ensured that no voltage is applied on any PWM pin on a non-powered module.

2.2.8 Analog Signals

The module provides two 12-bit Analog to Digital Converter (ADC). The following table shows the use of the ADC related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
M18	ADC_0	ADC_IN0	I	0 … 1.8 V	
N18	ADC_1	ADC_IN1	I	0 … 1.8 V	

Table 10: ADC (pin description)

2.2.9 SPI

The module provides two Serial Peripheral Interface (SPI) ports. The following table shows the use of the SPI related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
V15	SPI_A_SDO_(IO0)[1]	SD3_DATA0	I/O	1.8 V	
U15	SPI_A_SDI_(IO1)[1]	SD3_DATA1	I/O	1.8 V	
W16	SPI_A_WP_(IO2)[1]	SD3_DATA2	I/O	1.8 V	
W15	SPI_A_HOLD_(IO3)[1]	SD3_DATA3	I/O	1.8 V	
Y15	SPI_A_CS0#	SD3_CMD	O	1.8 V	
K17	SPI_A_CS1#	ENET2_MDC	O	1.8 V	dual function: GPIO_A_6
U16	SPI_A_SCK	SD3_CLK	O	1.8 V	
Y22	SPI_B_SDI	GPIO_IO09	I	1.8 V	
Y23	SPI_B_SDO	GPIO_IO10	O	1.8 V	

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AA23	SPI_B_CS0#	GPIO_IO08	O	1.8 V	
L17	SPI_B_CS1#	GPIO_IO24	O	1.8 V	dual function: GPIO_A_7
Y21	SPI_B_SCK	GPIO_IO11	O	1.8 V	

Table 11: SPI (pin description)

[1] F&S describes SPI_A as QuadSPI by default.

2.2.10 I2S

The module provides one Inter-IC Sound (I2S) interface. The following table shows the use of the I2S related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
V21	I2S_A_DATA_IN	GPIO_IO20	I	1.8 V	
W21	I2S_A_DATA_OUT	GPIO_IO21	O	1.8 V	
W18	I2S_A_LRCLK[1]	GPIO_IO26	I/O	1.8 V	
W20	I2S_A_BITCLK[1]	GPIO_IO16	I/O	1.8 V	
V18	I2S_MCLK	GPIO_IO17	O	1.8 V	

Table 12: I2S (pin description)

[1] Output, if module acts in Master Mode. Input, if module acts in Slave Mode.

2.2.11 CAN FD

The module provides two Controller Area Network Interfaces with Flexible Data-Rate (CAN FD). The following table shows the use of the CAN related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AC17	CAN_A_TX	PDM_CLK	O	1.8 V	
AB17	CAN_A_RX	PDM_BIT_STREAM0	I	1.8 V	
AC19	CAN_B_TX[1]	DAP_TDI	O	1.8 V	firmly connected to JTAG_TDI
AB19	CAN_B_RX[1]	DAP_TDO_TRACESWO	I	1.8 V	firmly connected to JTAG_TDO

Table 13: CAN FD (pin description)

[1] Do not use this function together with JTAG at the same time.

2.2.12 USB

The module provides two Universal Serial Busses (USB)[1], including controllers and PHYs. The following table shows the use of the USB related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AB13	USB_A_D_N	USB1_D_N	I/O	USB	
AC14	USB_A_D_P	USB1_D_P	I/O	USB	
AB14	USB_A_ID	USB1_ID	I	1.8 V	PU 10k
AC15	USB_A_OC#	PDM_BIT_STREAM1	I	1.8 V	PU 10k
AB16	USB_A_VBUS	USB1_VBUS	I	5.0 V	USB VBUS detection on the PHY port A[2]
AC16	USB_A_EN	GPIO_IO19	O	1.8 V	
AB23	USB_B_D_N	USB2_D_N	I/O	USB	
AC22	USB_B_D_P	USB2_D_P	I/O	USB	
AB22	USB_B_ID	USB2_ID	I	1.8 V	PU 10k
AC21	USB_B_OC#	GPIO_IO27	I	1.8 V	PU 10k
AB20	USB_B_VBUS	USB2_VBUS	I	5.0 V	USB VBUS detection on the PHY port B[2]
AC20	USB_B_EN	GPIO_IO18	O	1.8 V	

Table 14: USB (pin description)

[1] USB_A: USB 2.0 OTG & USB_B: USB 2.0 OTG.

[2] Must always be connected to the respective USB VBUS rail.

2.2.13 I2C

The module provides four Inter-Integrated Circuit (I2C) interfaces which are connected to the following components.

I2C	Connected To	Address	Comments
INT[1]	RTC	0x51	Real Time Clock on the module
	PMIC	0x25	Power Management IC on the module
A	EEPROM	0x50	EEPROM on the module (accessible from carrier)
	I2C_A		general I2C on carrier
B	I2C_B		general I2C on carrier
CAM	CAM_A_I2C		I2C, related to camera on carrier

Table 15: I2C (usage)

[1] I2C_INT is for internal use only.

The following table shows the use of the I2C related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AA15	I2C_A_SCL	I2C1_SCL	I/O	1.8 V	PU 2k2
AA16	I2C_A_SDA	I2C1_SDA	I/O	1.8 V	PU 2k2
AA20	I2C_B_SCL	GPIO_IO29	I/O	1.8 V	PU 2k2
AA21	I2C_B_SDA	GPIO_IO28	I/O	1.8 V	PU 2k2
C4	CAM_A_SCL	GPIO_IO23	I/O	1.8 V	PU 2k2
C3	CAM_A_SDA	GPIO_IO22	I/O	1.8 V	PU 2k2

Table 16: I2C (pin description)

2.2.14 PCIe

No Peripheral Component Interconnect (PCI) Express interface is implemented on the module.

2.2.15 MIPI CSI

The module provides one 2 lane Camera Serial Interface (CSI), defined by the Mobile Industry Processor Interface Alliance (MIPI):

- complaint with MIPI CSI-2 specification v1.3 and MIPI D-PHY specification v1.2.

The following table shows the use of the MIPI CSI related pins[1] on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
C1	CSI_A_DATA0_N	MIPI_CSI1_D0_N	I	MIPI CSI	
B1	CSI_A_DATA0_P	MIPI_CSI1_D0_P	I	MIPI CSI	
A2	CSI_A_DATA1_N	MIPI_CSI1_D1_N	I	MIPI CSI	
A3	CSI_A_DATA1_P	MIPI_CSI1_D1_P	I	MIPI CSI	
B3	CSI_A_CLOCK_N	MIPI_CSI1_CLOCK_N	I	MIPI CSI	
B4	CSI_A_CLOCK_P	MIPI_CSI1_CLOCK_P	I	MIPI CSI	
C2	CAM_MCK	CCM_CLKO1	O	1.8 V	
G3	CAM_A_PWR	CCM_CLKO2	O	1.8 V	dual function: GPIO_C_6
G4	CAM_A_RST#	CCM_CLKO3	O	1.8 V	dual function: GPIO_C_7

Table 17: CSI (pin description)

[1] CAM_A_I2C is described in the I2C chapter.

2.2.16 Display

Regarding the supported display (DISP) interface, the module is available in two versions[1]:

Version 1 single channel (4 lane) Low Voltage Differential Signal (LVDS) interface

Version 2 4 lane MIPI Display Serial Interface (DSI):

- complaint with MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2.

[1] Please contact sales@fs-net.de for further information.

The following table shows the use of the DISP related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AB11	DSI_DATA0_N LVDS_A_LANE0_N	MIPI_DSI_D0_N LVDS_D0_N	O	MIPI DSI LVDS	
AB10	DSI_DATA0_P LVDS_A_LANE0_P	MIPI_DSI_D0_P LVDS_D0_P	O	MIPI DSI LVDS	
AC9	DSI_DATA1_N LVDS_A_LANE1_N	MIPI_DSI_D1_N LVDS_D1_N	O	MIPI DSI LVDS	
AC8	DSI_DATA1_P LVDS_A_LANE1_P	MIPI_DSI_D1_P LVDS_D1_P	O	MIPI DSI LVDS	
AC6	DSI_DATA2_N LVDS_A_LANE2_N	MIPI_DSI_D2_N LVDS_D2_N	O	MIPI DSI LVDS	
AC5	DSI_DATA2_P LVDS_A_LANE2_P	MIPI_DSI_D2_P LVDS_D2_P	O	MIPI DSI LVDS	
AB5	DSI_DATA3_N LVDS_A_LANE3_N	MIPI_DSI_D3_N LVDS_D3_N	O	MIPI DSI LVDS	
AB4	DSI_DATA3_P LVDS_A_LANE3_P	MIPI_DSI_D3_P LVDS_D3_P	O	MIPI DSI LVDS	
AB8	DSI_CLOCK_N LVDS_A_CLK_N	MIPI_DSI_CLK_N LVDS_CLK_N	O	MIPI DSI LVDS	
AB7	DSI_ CLOCK _P LVDS_A_CLK_P	MIPI_DSI_CLK_P LVDS_CLK_P	O	MIPI DSI LVDS	
AA3	DSI_TE	CCM_CLKO4	O	1.8 V	DSI version: DSI panel tearing effect signal LVDS version: GPIO
F3	DISP_VDD_EN	ENET2_MDIO	O	1.8 V	dual function: GPIO_C_4
F4	DISP_BL_EN	GPIO_IO07	O	1.8 V	dual function: GPIO_C_5
E18	DISP_BL_PWM	GPIO_IO06	O	1.8 V	dual function: PWM_0

Table 18: DISP (pin description)

2.3 Internal Peripherals on the Module

2.3.1 LPDDR4

The module contains one 16-bit LPDDR4 SDRAM which operates with up to 3733 MT/s.

2.3.2 eMMC

The module contains one Embedded MultiMedia Card (eMMC) Flash memory. eMMCs have limited erasing cycles, and the data retention depends on the temperature. It is important to know that high temperatures above 50°C significantly impact the data retention of the eMMC[1], independently whether the device is powered or not.

[1] Please contact us for more information about data retention on eMMCs in high temperature environments.

2.3.3 RTC

The module contains a Real Time Clock (RTC, Type: PCF85263ATL)[1] which is connected to the internal I2C bus (I2C_INT, address: 0x51). The time can be maintained by applying a suitable voltage to V_RTC even if the module itself is not powered.

[1] Cause the accuracy is limited by the crystal, the RTC could drift some seconds per day.

2.3.4 EEPROM

The module contains a 64Kb Electrically Erasable Programmable Read-Only Memory (EEPROM) (Type: N24S64B) which is connected to I2C_A (address: 0x50).

3 Characteristics

3.1 Absolute Maximum Ratings[1]

Parameter	Description	Min	Max	Unit
V_{5V}	main power input voltage at the V_5V_IN pins	-0.50	6.00	V
V_{RTC}	RTC battery input voltage at the RTC_PWR pin	-0.50	6.50	V
V_{IO}	general I/O voltage (V_{DD} … nominal I/O voltage)	-0.30	V_{DD} + 0.30	V
USB VBUS	PHY detection signal of USB port supply voltage on the carrier	-0.30	5.50	V

Table 19: Absolute Maximum Ratings

[1] Stresses beyond the listed values may affect reliability or cause permanent damage to the module.

3.2 Recommended Operating Conditions

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{5V}	main power input[1]		4.50	5.00	5.50	V
I_{5V}					1.5	A
V_{RTC}	RTC battery input	contact: **W17** V_{RTC} = 3.0 V	1.20	3.00	5.50	V
I_{RTC}				350	480	nA
USB VBUS	PHY detection of USB VBUS	contact: **AB16, AB20**		5.00		V
$V_{VCC\_2\_TEST}$	supply output (for testing purposes)	contact: **M19**		1.80		V
$I_{VCC\_2\_TEST}$					50	mA
$V_{VCC\_4\_TEST}$	supply output (for carrier peripherals)	contact: **Y20**		3.30		V
$I_{VCC\_4\_TEST}$					200	mA
$V_{VCC\_OUT\_IO}$	supply output (general I/O reference)	contact: **U18**		1.80		V
$I_{VCC\_OUT\_IO}$					100	mA
V_{ETH_IOPWR}	supply output (Ethernet I/O reference)	contact: **M17**		1.80		V
I_{ETH_IOPWR}					100	mA
$V_{SDIO\_A\_IOPWR}$	supply output (SDIO_A I/O reference)	contact: **C20**		1.80	3.30	V
$I_{SDIO\_A\_IOPWR}$					100	mA
V_{IH}	I/O high-level input voltage	V_{DD} = 1.8 V / 3.3 V	0.7 · V_{DD}	V_{DD}	V_{DD} + 0.2	V
V_{IL}	I/O low-level I/O input voltage		-0.20		0.3 · V_{DD}	V
V_{OH}	I/O high-level output voltage		0.8 · V_{DD}		V_{DD}	V
V_{OL}	I/O low-level I/O output voltage		0		0.2 · V_{DD}	V
I_{GPIO_OUT}	I/O drive strength (general)				8	mA
V_{ADC_IN}	ADC input voltage range		0		1.80	V
$T_{OPERATE}$	operating temperature range[2]	C TEMP grade	0		70	°C
		I TEMP grade	-25		85	°C
		XI TEMP grade	-40		85	°C
$T_{STORAGE}$	storage temperature range		-40		85	°C
$t_{STORAGE}$	storage time	no environmental control		6	months	
		T_{AMB} = 25 °C ± 5 °C humidity max. 60 %		12	months	

Table 20: Recommended Operating Conditions

[1] The OSM standard requires 5.0 V ± 5 %, but the module is tested and validated within the specified range.

[2] An external cooling solution may be required to cover the entire range.

4 Packaging & Labels

4.1 ESD

All F&S electrostatic discharge sensitive (ESDS) products are marked and will be shipped in ESD protective packaging.

4.2 Serial Number

All shipped F&S products are labeled with a matrix code sticker that includes the serial number. For product information visit www.fsembedded.com/en/support/serial-number-info-and-rma/.

5 Appendix

5.1 Second source rules

The qualifications of products from a second source are done autonomously by F&S. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible. F&S does not use broker components without the consent of the customer.

5.2 RoHS and REACH statement

Please see the following webpage: www.fsembedded.com/en/support/certifications/

5.3 Important Notice

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