Hardware Documentation

PicoCore™MX8MP
for HW Revision 1.00

Version 007
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© F&S Elektronik Systeme GmbH
Untere Waldplätze 23
D-70569 Stuttgart
Phone: +49(0)711-123722-0
Fax: +49(0)711-123722-99

About This Document

This document describes how to use the PicoCore™MX8MP board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

This document is written for the PicoCoreMX8MP which are given in the table below.

Related Modules
PicoCore™MX8MP-V1-LIN
PicoCore™MX8MP-V2-LIN
PicoCore™MX8MP-V3I-LIN
PicoCore™MX8MP-V3XI-LIN
PicoCore™MX8MP-V4I-LIN
PicoCore™MX8MP-V4XI-LIN

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
22.03.2021	001	All		-	Initial Version	MD
19.05.2021	002	All	M	3.1, 4.6	Minor Corrections	MD
08.07.2021	003	All	M	3.1, 4.8	Corrections on Audio_B Signals	MD
02.11.2021	004	All	M M A	9, 13 4.8 2.2	Updates on the thermal specifications Minor corrections on Table 12 in the Audio Chapter Addition of the *Heat Spreader* section	MD
19.01.2023	005	All	A	8.1	Absolute maximum ratings of 1.8V I/Os added.	UK
29.01.2024	006	All	A M M	4.16 4.1 13	New chapter Boot-Mode Correct remark for USB_HOST_VBUS Change text	DB SM
17.10.2025	007	All	M	3.1	Correct Text for I2C_D	MW

V Version
A,M,R Added, Modified, Removed
Au Author

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1 Block diagram

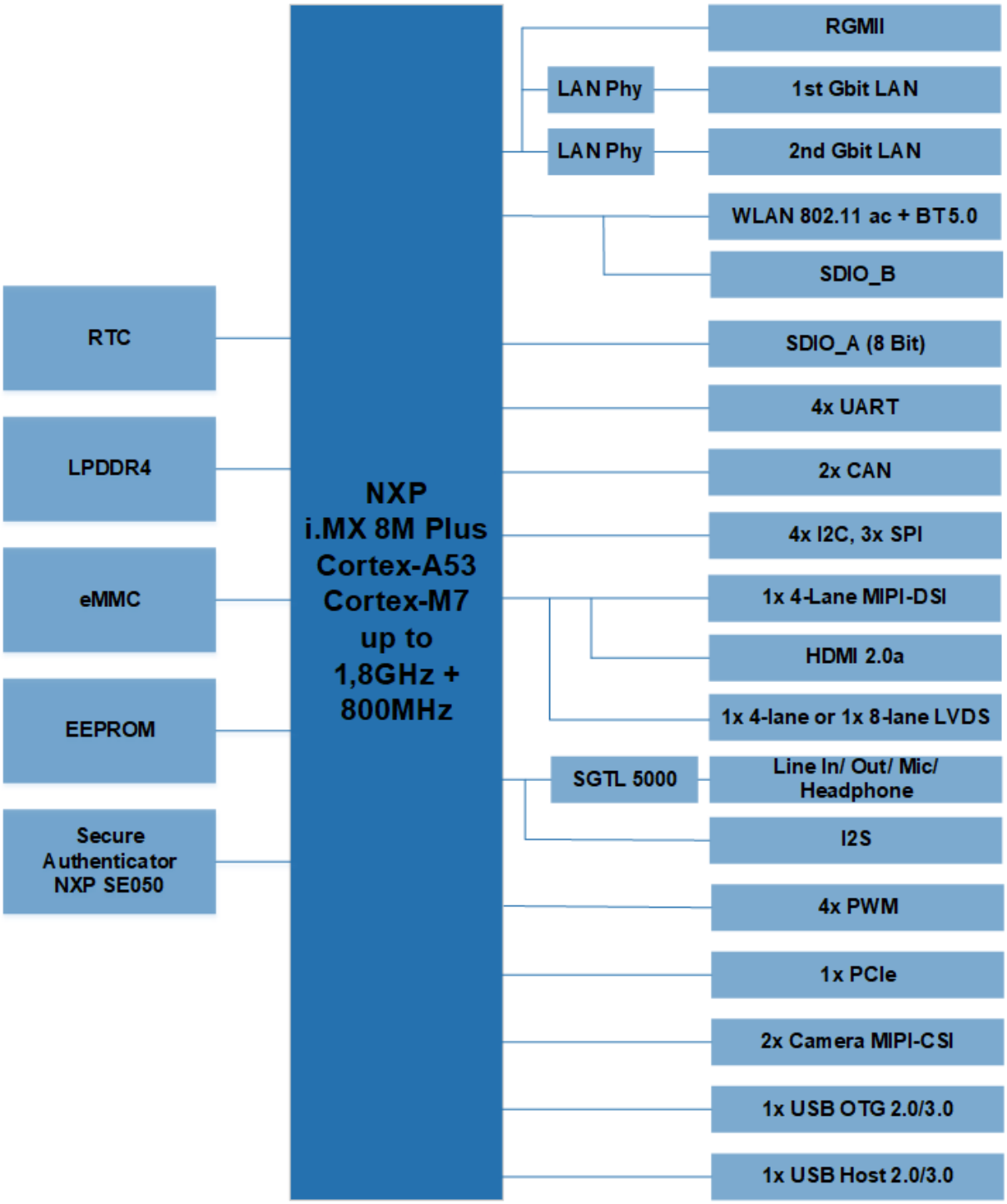

Figure 1: Block Diagram

2 Mechanical Dimension

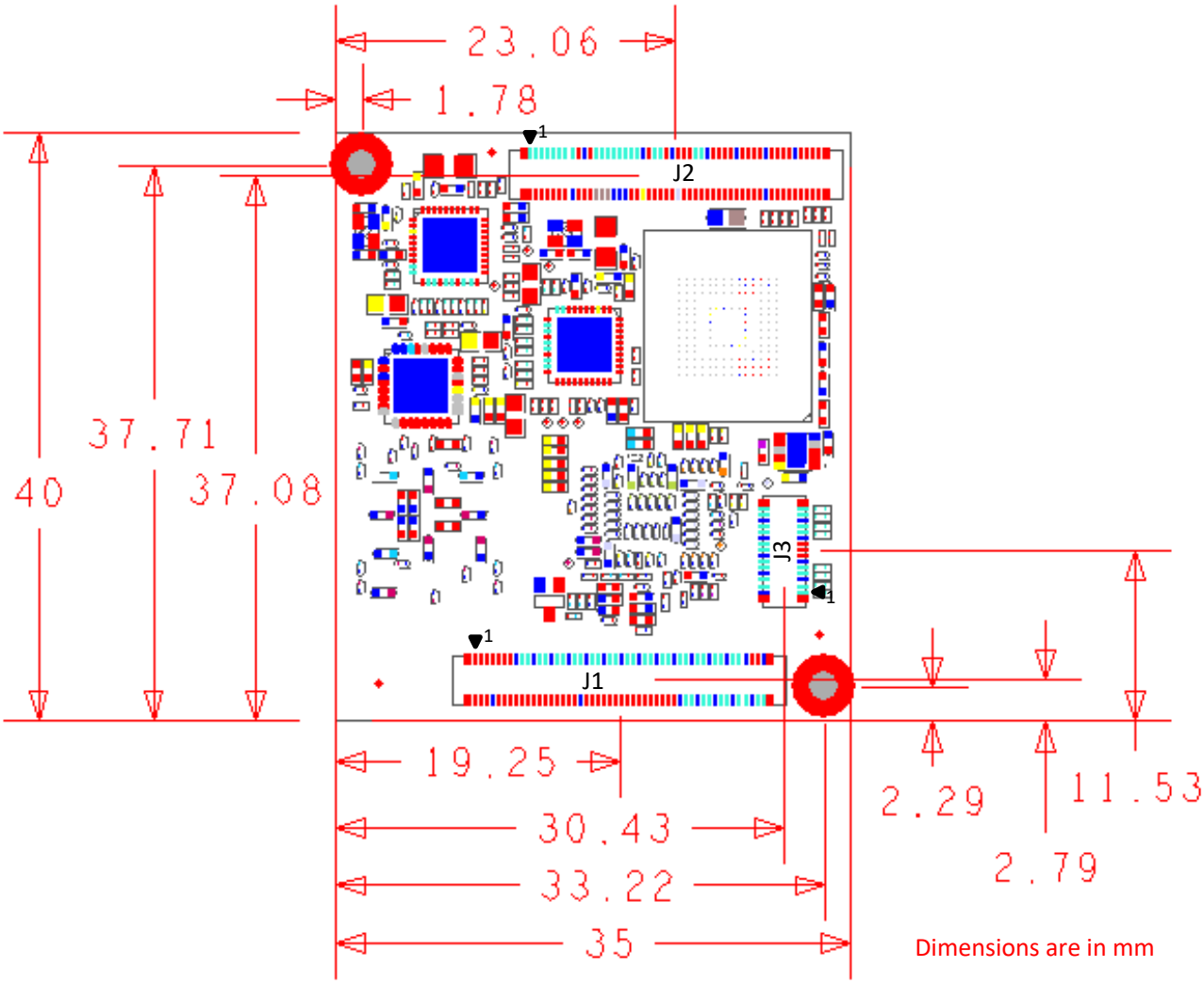

Figure 2: Mechanical Dimension from bottom side (dimensions in imm)

Dimensions	Description
Size	40mm x 35mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	Max. 5mm
Height of the parts on the bottom side	Max. 1.4mm
Weight	14gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

2.1 SMT Steel Spacer

For mounting we recommend SMT Steel Spacer components, order number **B.MSCHR.22.** This part is in F&S stock and can be ordered via F&S web shop.

The stack height of the space is 1.5mm. If a different stack height is needed, another spacer should be chosen.

Data sheet and 3D model (STP) is available on our website.

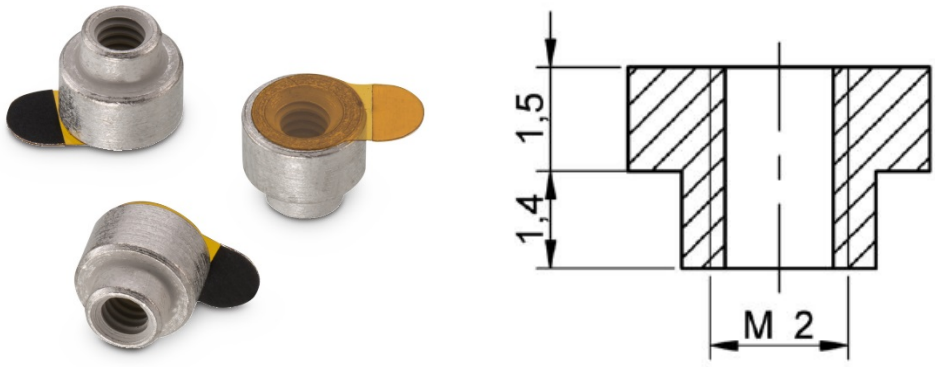

Figure 3: SMT Steel Spacer

2.2 Heat Spreader

As a base for the cooling concept, F&S offers a heat spreader. Part number of heat spreader is **MHS.PC100.1** and can be ordered via F&S web shop.

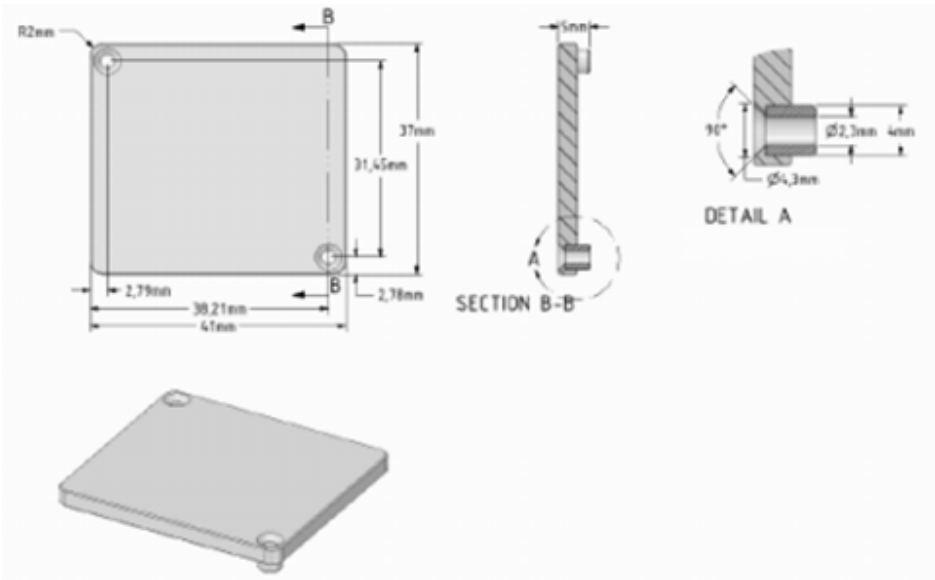

Figure 4: Heat Spreader (Images are not to scale)

3 Interface and signal description

3.1 B2B connectors

PicoCoreMX8MP is using two 100 pin connectors (J1/J2) and one 30 pin (J3) connector from manufacturer Hirose.

Part number J1/J2: DF40C-100DP-0.4V.

Part number for the counterpart *J1/J2*: DF40C-100DS-0.4V

Part number J3: DF40C-30DP-0.4V.

Part number for the counterpart *J3*: DF40C-30DS-0.4V

With this combination you get minimal stacking height of 1,5mm. Other possible stacking height by using different counterpart connector is: 3mm. The connector with 1,5mm stacking height is available at F&S and can be ordered in web shop.

Connector J1/J2 is compatible to J1/J2 of PicoCoreMX8MM (NXP i.MX8M Mini) and PicoCoreMX8MN (NXP i.MX8M Nano) and PicoCoreMX6UL100 (NXP i.MX6UL).

Connector J3 is optional and only mounted in configurations with USB 3.0 and 2x MIPI-CSI.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
			J1			
J1	1	I2C_B_IRQ	GPIO1_IO13	I	3.3V	I2C_B Interrupt
J1	2	GPIO_J1_2	GPIO1_IO15	I/O	3.3V	Standard GPIO
J1	3	I2C_B_SCL	I2C4_SCL	O	3.3V	I2C_B Serial Clock
J1	4	I2C_A_SCL	HDMI_HPD	O	3.3V	I2C_A Serial Clock
J1	5	I2C_B_SDA	I2C4_SDA	I/O	3.3V	I2C_B Serial Data
J1	6	I2C_A_SDA	HDMI_CEC	I/O	3.3V	I2C_A Serial Data
J1	7	GPIO_J1_7	SPDIF_EXT_CLK	I/O	3.3V	Standard GPIO
J1	8	GND		PWR	GND	
J1	9	BL_ON	SPDIF_TX	O	3.3V	Backlight Enable
J1	10	CAN_A_RX	HDMI_DDC_SDA	I	3.3V	CAN_A Data Receive
J1	11	BL_PWM	SPDIF_RX	O	3.3V	Backlight PWM
J1	12	CAN_A_TX	HDMI_DDC_SCL	O	3.3V	CAN_A Data Transmit
J1	13	VLCD_ON	SAI3_MCLK	O	3.3V	VLCD Enable
J1	14	UART_A_RTS	UART4_RXD	O	3.3V	UART_A Ready to Send
J1	15	GND		PWR	GND	
J1	16	UART_A_CTS	UART4_TXD	I	3.3V	UART_A Clear to Send
J1	17	DSI_A_CLK_P	MIPI_DSI1_CLK_P LVDS0_CLK_P	O	1.8V	MIPI-DSI Clock+ LVDS0 Clock+
J1	18	UART_A_RXD	SAI3_TXFS	I	3.3V	UART_A Data Receive
J1	19	DSI_A_CLK_N	MIPI_DSI1_CLK_N LVDS0_CLK_N	O	1.8V	MIPI-DSI Clock- LVDS0 Clock-
J1	20	UART_A_TXD	SAI3_TXC	O	3.3V	UART_A Data Transmit

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	21	GND		PWR	GND	
J1	22	UART_B_RTS	NAND_DATA02	O	3.3V	UART_B Ready to Send
J1	23	DSI_A_DATA0_P	MIPI_DSI1_D0_P LVDS0_D0_P	O	1.8V	MIPI-DSI Data0+ LVDS0 Data0+
J1	24	UART_B_CTS	NAND_DATA03	I	3.3V	UART_B Clear to Send
J1	25	DSI_A_DATA0_N	MIPI_DSI1_D0_N LVDS0_D0_N	O	1.8V	MIPI-DSI Data0- LVDS0 Data0-
J1	26	UART_B_RXD	NAND_DATA00	I	3.3V	UART_B Data Receive
J1	27	GND		PWR	GND	
J1	28	UART_B_TXD	NAND_DATA01	O	3.3V	UART_B Data Transmit
J1	29	DSI_A_DATA1_P	MIPI_DSI1_D1_P LVDS0_D1_P	O	1.8V	MIPI-DSI Data1+ LVDS0 Data1+
J1	30	UART_C_RXD	SAI2_RXC	I	3.3V	UART_C Data Receive
J1	31	DSI_A_DATA1_N	MIPI_DSI1_D1_N LVDS0_D1_N	O	1.8V	MIPI-DSI Data1- LVDS0 Data1-
J1	32	UART_C_TXD	SAI2_RXFS	O	3.3V	UART_C Data Transmit
J1	33	GND		PWR	GND	
J1	34	UART_D_RXD	UART3_RXD	I	3.3V	UART_D Data Receive
J1	35	DSI_A_DATA2_P	MIPI_DSI1_D2_P LVDS0_D2_P	O	1.8V	MIPI-DSI Data2+ LVDS0 Data2+
J1	36	UART_D_TXD	UART3_TXD	O	3.3V	UART_D Data Transmit
J1	37	DSI_A_DATA2_N	MIPI_DSI1_D2_N LVDS0_D2_N	O	1.8V	MIPI-DSI Data2- LVDS0 Data2-
J1	38	GND		PWR	GND	
J1	39	GND		PWR	GND	
J1	40	I2C_C_SCL	ECSPI1_MISO	O	3.3V	I2C_C Serial Clock
J1	41	DSI_A_DATA3_P	MIPI_DSI1_D3_P LVDS0_D3_P	O	1.8V	MIPI-DSI Data3+ LVDS0 Data3+
J1	42	I2C_C_SDA	ECSPI1_SS0	I/O	3.3V	I2C_C Serial Data
J1	43	DSI_A_DATA3_N	MIPI_DSI1_D3_N LVDS0_D3_N	O	1.8V	MIPI-DSI Data3- LVDS0 Data3-
J1	44	GPIO_J1_44	NAND_ALE	I/O	3.3V	Standard GPIO
J1	45	GND		PWR	GND	
J1	46	GPIO_J1_46	NAND_CE0_B	I/O	3.3V	Standard GPIO
J1	47	DSI_B_CLK_P*[3]	HDMI_TXC_P LVDS1_CLK_P	O	1.8V	HDMI TX Clock+ LVDS1 Clock+
J1	48	I2C_D_SCL	I2C3_SCL	O	3.3V	I2C_D Serial Clock
J1	49	DSI_B_CLK_N	HDMI_TXC_N LVDS1_CLK_N	O	1.8V	HDMI TX Clock- LVDS1 Clock-
J1	50	I2C_D_SDA	I2C3_SDA	I/O	3.3V	I2C_D Serial Data
J1	51	GND		PWR	GND	
J1	52	GPIO_J1_52	NAND_DQS	I/O	3.3V	Standard GPIO

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	53	DSI_B_DATA0_P	HDMI_TX0_P LVDS1_D0_P	O	1.8V	HDMI TX Data0+ LVDS1 Data0+
J1	54	GPIO_J1_54	GPIO1_IO01	I/O	3.3V	Standard GPIO
J1	55	DSI_B_DATA0_N	HDMI_TX0_N LVDS1_D0_N	O	1.8V	HDMI TX Data0- LVDS1 Data0-
J1	56	SPI_B_SS0	ECSPI2_SS0	I/O	3.3V	SPI_B Slave Select
J1	57	GND		PWR	GND	
J1	58	SPI_B_MISO	ECSPI2_MISO	I/O	3.3V	SPI_B Master In-Slave Out
J1	59	DSI_B_DATA1_P	HDMI_TX1_P LVDS1_D1_P	O	1.8V	HDMI TX Data1+ LVDS1 Data1+
J1	60	SPI_B_MOSI	ECSPI2_MOSI	I/O	3.3V	SPI_B Master Out-Slave In
J1	61	DSI_B_DATA1_N	HDMI_TX1_N LVDS1_D1_N	O	1.8V	HDMI TX Data1- LVDS1 Data1-
J1	62	SPI_B_SCLK	ECSPI2_SCLK	I/O	3.3V	SPI_B Serial Clock
J1	63	GND		PWR	GND	
J1	64	SPI_A_SS0	UART2_TXD	I/O	3.3V	SPI_A Slave Select
J1	65	DSI_B_DATA2_P	HDMI_TX2_P LVDS1_D2_P	O	1.8V	HDMI TX Data2+ LVDS1 Data2+
J1	66	SPI_A_MISO	UART2_RXD	I/O	3.3V	SPI_A Master In-Slave Out
J1	67	DSI_B_DATA2_N	HDMI_TX2_N LVDS1_D2_N	O	1.8V	HDMI TX Data2- LVDS1 Data2-
J1	68	SPI_A_MOSI	UART1_TXD	I/O	3.3V	SPI_A Master Out-Slave In
J1	69	GND		PWR	GND	
J1	70	SPI_A_SCLK	UART1_RXD	O	3.3V	SPI_A Serial Clock
J1	71	DSI_B_DATA3_P	HDMI_TX3_P LVDS1_D3_P	O	1.8V	HDMI TX Data3+ LVDS1 Data3+
J1	72	GND		PWR	GND	
J1	73	DSI_B_DATA3_N	HDMI_TX3_N LVDS1_D3_N	O	1.8V	HDMI TX Data3- LVDS1 Data3-
J1	74	CSI_A_CLK_P	MIPI_CSI1_CLK_P	I	1.8V	CSI_A Input Clock+
J1	75	GND		PWR	GND	
J1	76	CSI_A_CLK_N	MIPI_CSI1_CLK_N	I	1.8V	CSI_A Input Clock-
J1	77	MPCIE_CTX_P	PCIE_TXN_P	O	1.8V	mPCIe Transmit Data+
J1	78	GND		PWR	GND	
J1	79	MPCIE_CTX_N	PCIE_TXN_N	O	1.8V	mPCIe Transmit Data-
J1	80	CSI_A_DATA0_P	MIPI_CSI1_D0_P	I	1.8V	CSI_A Input Data0+
J1	81	GND		PWR	GND	
J1	82	CSI_A_DATA0_N	MIPI_CSI1_D0_N	I	1.8V	CSI_A Input Data0-
J1	83	MPCIE_CRX_P	PCIE_RXN_P	I	1.8V	mPCIe Receive Data+
J1	84	GND		PWR	GND	
J1	85	MPCIE_CRX_N	PCIE_RXN_N	I	1.8V	mPCIe Receive Data-
J1	86	CSI_A_DATA1_P	MIPI_CSI1_D1_P	I	1.8V	CSI_A Input Data1+

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	87	GND		PWR	GND	
J1	88	CSI_A_DATA1_N	MIPI_CSI1_D1_N	I	1.8V	CSI_A Input Data1-
J1	89	MPCIE_CLK_P	PCIE_REF_PAD_CLK_P	O	1.8V	mPCIe Clock+
J1	90	GND		PWR	GND	
J1	91	MPCIE_CLK_N	PCIE_REF_PAD_CLK_N	O	1.8V	mPCIe Clock-
J1	92	CSI_A_DATA2_P	MIPI_CSI1_D2_P	I	1.8V	CSI_A Input Data2+
J1	93	GND		PWR	GND	
J1	94	CSI_A_DATA2_N	MIPI_CSI1_D2_N	I	1.8V	CSI_A Input Data2-
J1	95	MPCIE_PERST	SAI3_RXD	O	3.3V	mPCIe Power Reset
J1	96	GND		PWR	GND	
J1	97	MPCIE_WAKE	SAI3_TXD	I	3.3V	mPCIe Wake
J1	98	CSI_A_DATA3_P	MIPI_CSI1_D3_P	I	1.8V	CSI_A Input Data3+
J1	99	GND		PWR	GND	
J1	100	CSI_A_DATA3_N	MIPI_CSI1_D3_N	I	1.8V	CSI_A Input Data3-
J2						
J2	1	ETH_A_D1P		I/O	1.2V/1.8V	ETH_A PHY Data1+
J2	2	AUDIO_A_VCC		PWR	3V/3.3V	Audio Supply Voltage
J2	3	ETH_A_D1N		I/O	1.2V/1.8V	ETH_A PHY Data1-
J2	4	AUDIO_A_GND		PWR	GND	Audio GND
J2	5	ETH_A_D2P		I/O	1.2V/1.8V	ETH_A PHY Data2+
J2	6	AUDIO_A_LOUT_L		O	-	Line Out Left
J2	7	ETH_A_D2N		I/O	1.2V/1.8V	ETH_A PHY Data2-
J2	8	AUDIO_A_LOUT_R		O	-	Line Out Right
J2	9	ETH_A_D3P		I/O	1.2V/1.8V	ETH_A PHY Data3+
J2	10	AUDIO_A_MIC		I	-	Microphone In
J2	11	ETH_A_D3N		I/O	1.2V/1.8V	ETH_A PHY Data3-
J2	12	AUDIO_A_LIN_L		I	-	Line In Left
J2	13	ETH_A_D4P		I/O	1.2V/1.8V	ETH_A PHY Data4+
J2	14	AUDIO_A_LIN_R		I	-	Line In Right
J2	15	ETH_A_D4N		I/O	1.2V/1.8V	ETH_A PHY Data4-
J2	16	GND		PWR	GND	
J2	17	ETH_A_LED		O	2.5V	ETH_A PHY Activity LED
J2	18	AUDIO_A_HP_L		O	-	Headphone Out Left
J2	19	GND		PWR	GND	
J2	20	AUDIO_A_HP_R		O	-	Headphone Out Right
J2	21	ETH_B_LED		O	2.5V	ETH_B PHY Activity LED
J2	22	AUDIO_A_HP_GND		O	GND	Headphone GND
J2	23	ETH_B_D1P		I/O	1.2V/1.8V	ETH_A PHY Data1+

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	24	VDD_VIN		PWR	5.0V	Supply Voltage Input
J2	25	ETH_B_D1N		I/O	1.2V/1.8V	ETH_A PHY Data1-
J2	26	VDD_VIN		PWR	5.0V	Supply Voltage Input
J2	27	ETH_B_D2P		I/O	1.2V/1.8V	ETH_A PHY Data2+
J2	28	VDD_VIN		PWR	5.0V	Supply Voltage Input
J2	29	ETH_B_D2N		I/O	1.2V/1.8V	ETH_A PHY Data2-
J2	30	GND		PWR	GND	
J2	31	ETH_B_D3P		I/O	1.2V/1.8V	ETH_A PHY Data3+
J2	32	GND		PWR	GND	
J2	33	ETH_B_D3N		I/O	1.2V/1.8V	ETH_A PHY Data3-
J2	34	GND		PWR	GND	
J2	35	ETH_B_D4P		I/O	1.2V/1.8V	ETH_A PHY Data4+
J2	36	VDD_VBAT		PWR	0.9V ~ 5.5V	RTC Battery Backup Supply Voltage
J2	37	ETH_B_D4N		I/O	1.2V/1.8V	ETH_A PHY Data4+
J2	38	RESERVED		X		N.C.
J2	39	GND		PWR	GND	
J2	40	VDD_3V3		O	3.3V	20mA output from on module DCDC powered from VIN
J2	41	USB_HOST_VBUS	USB1_VBUS	PWR	5.0V	USB Host VBUS Input
J2	42	RESETINN		I	1.8V	Reset Input for PMIC
J2	43	USB_HOST_DP	USB1_D_P	I/O	3.3V	USB Host Data+
J2	44	PMIC_STBY	PMIC_STBY_REQ	O	1.8V	PMIC Standby
J2	45	USB_HOST_DN	USB1_D_N	I/O	3.3V	USB Host Data-
J2	46	PMIC_ON_REQ	PMIC_ON_REQ	O	1.8V	PMIC On
J2	47	USB_HOST_PWR	GPIO1_IO12	O	3.3V	USB Host Power Enable
J2	48	ON_OFF	ONOFF	I	1.8V	On/Off Input for CPU
J2	49	GND		PWR	GND	
J2	50	BOOTSEL		I	1.8V	Service jumper; normally left open
J2	51	USB_OTG_VBUS	USB2_VBUS	PWR	5.0V	USB OTG VBUS Input
J2	52	SD_A_VCC		O	1.8V/3.3V	SD_A Supply Voltage, 150mA max Output
J2	53	USB_OTG_PWR	GPIO1_IO14	O	3.3V	USB OTG Power Enable
J2	54	SD_A_STROBE	SD1_STROBE	O	SD_A_VCC	SD_A Strobe
J2	55	USB_OTG_ID	USB2_ID	I	3.3V	USB OTG ID
J2	56	SD_A_RST	SD1_RESET_B	O	SD_A_VCC	SD_A Reset
J2	57	USB_OTG_DP	USB2_D_P	I/O	3.3V	USB OTG Data+
J2	58	SD_A_WP	GPIO1_IO07	I	3.3V	SD_A Write Protect

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	59	USB_OTG_DN	USB2_D_N	I/O	3.3V	USB OTG Data-
J2	60	SD_A_CD	GPIO1_IO06	I	3.3V	SD_A Card Detect
J2	61	GND		PWR	GND	
J2	62	SD_A_CMD	SD1_CMD	O	SD_A_VCC	SD_A Command
J2	63	PWM	GPIO1_IO10	O	3.3V	PWM Output
J2	64	SD_A_CLK	SD1_CLK	O	SD_A_VCC	SD_A Clock
J2	65	AUDIO_B_I2S_MCLK	SAI1_MCLK	O	1.8V	*See chapter 4.8
J2	66	SD_A_DATA0	SD1_DATA0	I/O	SD_A_VCC	SD_A Data0
J2	67	AUDIO_B_I2S_TXFS	SAI5_TXFS	I/O	1.8V	*See chapter 4.8
J2	68	SD_A_DATA1	SD1_DATA1	I/O	SD_A_VCC	SD_A Data1
J2	69	AUDIO_B_I2S_TXC	SAI5_TXC	O	1.8V	*See chapter 4.8
J2	70	SD_A_DATA2	SD1_DATA2	I/O	SD_A_VCC	SD_A Data2
J2	71	GND		PWR	GND	
J2	72	SD_A_DATA3	SD1_DATA3	I/O	SD_A_VCC	SD_A Data3
J2	73	AUDIO_B_I2S_TXD	SAI5_TXD0	O	1.8V	*See chapter 4.8
J2	74	SD_A_DATA4	SD1_DATA4	I/O	SD_A_VCC	SD_A Data4
J2	75	AUDIO_B_I2S_RXD	SAI1_RXD0	I	1.8V	*See chapter 4.8
J2	76	SD_A_DATA5	SD1_DATA5	I/O	SD_A_VCC	SD_A Data5
J2	77	AUDIO_B_I2S_RXFS	SAI5_RXFS	I/O	1.8V	*See chapter 4.8
J2	78	SD_A_DATA6	SD1_DATA6	I/O	SD_A_VCC	SD_A Data6
J2	79	AUDIO_B_I2S_RXC	SAI5_RXC	I	1.8V	*See chapter 4.8
J2	80	SD_A_DATA7	SD1_DATA7	I/O	SD_A_VCC	SD_A Data7
J2	81	GND		PWR	GND	
J2	82	GND		PWR	GND	
J2	83	SPI_C_SS0	I2C2_SDA	I/O	3.3V	SPI_C Slave Select
J2	84	SD_B_RST	SD2_RESET_B	O	SD_B_VCC	SD_B Reset
J2	85	SPI_C_MISO	I2C2_SCL	I/O	3.3V	SPI_C Master In-Slave Out
J2	86	SD_B_WP	SD2_WP	I	SD_B_VCC	SD_B Write Protect
J2	87	SPI_C_MOSI	ECSPI1_MOSI	I/O	3.3V	SPI_C Master Out-Slave In
J2	88	SD_B_CD	SD2_CD_B	I	SD_B_VCC	SD_B Card Detect
J2	89	SPI_C_SCLK	ECSPI1_SCLK	I/O	3.3V	SPI_C Serial Clock
J2	90	SD_B_CMD	SD2_CMD	O	SD_B_VCC	SD_B Command
J2	91	GND		PWR	GND	
J2	92	SD_B_CLK	SD2_CLK	O	SD_B_VCC	SD_B Command
J2	93	JTAG_TCK	JTAG_TCK	I	1.8V	JTAG Test Clock
J2	94	SD_B_DATA0	SD2_DATA0	I/O	SD_B_VCC	SD_B Data0
J2	95	JTAG_TMS	JTAG_TMS	I	1.8V	JTAG Test Mode Select
J2	96	SD_B_DATA1	SD2_DATA1	I/O	SD_B_VCC	SD_B Data1

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	97	JTAG_TDI	JTAG_TDI	I	1.8V	JTAG Test Data In
J2	98	SD_B_DATA2	SD2_DATA2	I/O	SD_B_VCC	SD_B Data2
J2	99	JTAG_TDO	JTAG_TDO	O	1.8V	JTAG Test Data Out
J2	100	SD_B_DATA3	SD2_DATA3	I/O	SD_B_VCC	SD_B Data3
			J3			
J3	1	USB_HOST_SS_RXP	USB1_RX_P	I	3.3V	USB Host 3.0 RX Data+
J3	2	GND		PWR	GND	
J3	3	USB_HOST_SS_RXN	USB1_RX_N	I	3.3V	USB Host 3.0 RX Data-
J3	4	CSI_B_CLK_P	MIPI_CSI2_CLK_P	I	1.8V	CSI_B Input Clock+
J3	5	GND		PWR	GND	
J3	6	CSI_B_CLK_N	MIPI_CSI2_CLK_N	I	1.8V	CSI_B Input Clock-
J3	7	USB_HOST_SS_TXP	USB1_TX_P	O	3.3V	USB Host 3.0 TX Data+
J3	8	GND		PWR	GND	
J3	9	USB_HOST_SS_TXN	USB1_TX_N	O	3.3V	USB Host 3.0 TX Data-
J3	10	CSI_B_DATA0_P	MIPI_CSI2_D0_P	I	1.8V	CSI_B Input Data0+
J3	11	GND		PWR	GND	
J3	12	CSI_B_DATA0_N	MIPI_CSI2_D0_N	I	1.8V	CSI_B Input Data0-
J3	13	USB_TYPEC_EN	GPIO1_IO05	I/O	3.3V	USB OTG Type C Enable
J3	14	GND		PWR	GND	
J3	15	USB_TYPEC_ALERT	GPIO1_IO08	I/O	3.3V	USB OTG Type C Alert
J3	16	CSI_B_DATA1_P	MIPI_CSI2_D1_P	I	1.8V	CSI_B Input Data1+
J3	17	USB_TYPEC_SEL	GPIO1_IO09	I/O	3.3V	USB OTG Type C Select
J3	18	CSI_B_DATA1_N	MIPI_CSI2_D1_N	I	1.8V	CSI_B Input Data1-
J3	19	GND			GND	
J3	20	GND			GND	
J3	21	USB_OTG_SS_RXP	USB2_RX_P	I	3.3V	USB OTG 3.0 RX Data+
J3	22	CSI_B_DATA2_P	MIPI_CSI2_D2_P	I	1.8V	CSI_B Input Data2+
J3	23	USB_OTG_SS_RXN	USB2_RX_N	I	3.3V	USB OTG 3.0 RX Data-
J3	24	CSI_B_DATA2_N	MIPI_CSI2_D2_N	I	1.8V	CSI_B Input Data2-
J3	25	GND		PWR	GND	
J3	26	GND		PWR	GND	
J3	27	USB_OTG_SS_TXP	USB2_TX_P	O	3.3V	USB OTG 3.0 TX Data+
J3	28	CSI_B_DATA3_P	MIPI_CSI2_D3_P	I	1.8V	CSI_B Input Data3+
J3	29	USB_OTG_SS_TXN	USB2_TX_N	O	3.3V	USB OTG 3.0 TX Data-
J3	30	CSI_B_DATA3_N	MIPI_CSI2_D3_N	I	1.8V	CSI_B Input Data3-

Table 2: B2B connector

4 Interfaces

4.1 USB Interface (2.0 & 3.0)

PicoCoreMX8MP module can support 1x USB 2.0/3.0 Host and 1x USB 2.0/3.0 OTG. The USB OTG can also support USB-Type C connection. The high speed USB 3.0 and Type-C connection are optional and do not come with the standard configuration.

The 90 Ohm differential pairs of USB signals need no termination.

For external ports ESD and EMV protection is required nearby the USB connectors.

If the USB OTG will be used in Host Mode, the **USB_OTG_ID** pin should be pulled down to GND with a resistor. Otherwise it must be directly connected to the USB connector.

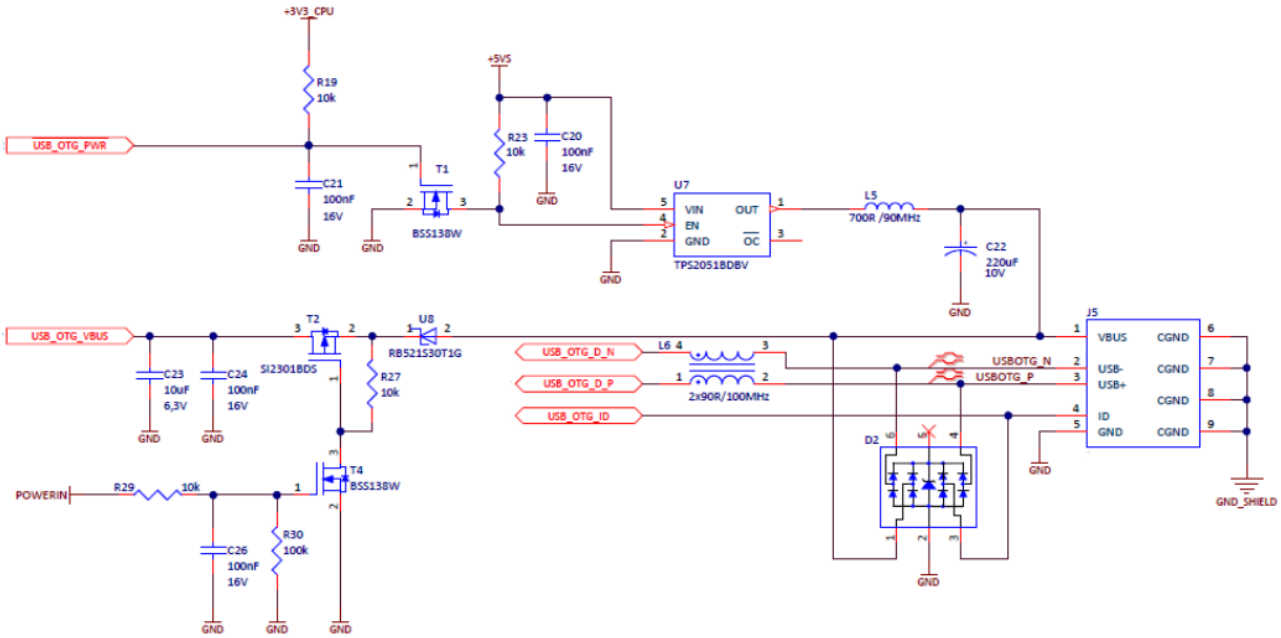

Figure 5: USB OTG example connection

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
USB Host 2.0 [USB 3.0 optional]						
J2	41	USB_HOST_VBUS	USB1_VBUS	I	5.0V	USB Host voltage detection
J2	43	USB_HOST_DP	USB1_D_P	I/O	3.3V	90Ohm differential pair
J2	45	USB_HOST_DN	USB1_D_N	I/O	3.3V	90Ohm differential pair
J2	47	USB_HOST_PWR	GPIO1_IO12	O	3.3V	**No pull-up/down on module**
J3	1	USB_HOST_SS_RXP	USB1_RX_P	I	3.3V	90Ohm differential pair
J3	3	USB_HOST_SS_RXN	USB1_RX_N	I	3.3V	90Ohm differential pair
J3	7	USB_HOST_SS_TXP	USB1_TX_P	O	3.3V	90Ohm differential pair
J3	9	USB_HOST_SS_TXN	USB1_TX_N	O	3.3V	90Ohm differential pair
USB OTG 2.0 [USB 3.0 optional]						
J2	51	USB_OTG_VBUS	USB2_VBUS	I	5.0V	USB OTG Voltage detection
J2	53	USB_OTG_PWR	GPIO1_IO14	O	3.3V	**No pull-up/down on module**
J2	55	USB_OTG_ID	USB2_ID	I	3.3V	Should be pulled down to GND for Host Mode, otherwise connect directly to the connector
J2	57	USB_OTG_DP	USB2_D_P	I/O	3.3V	90Ohm differential pair
J2	59	USB_OTG_DN	USB2_D_N	I/O	3.3V	90Ohm differential pair
J3	13	USB_OTG_TYPEC_EN	GPIO1_IO05	O	3.3V	**No pull-up/down on module**
J3	15	USB_OTG_TYPEC_ALERT	GPIO1_IO08	O	3.3V	**No pull-up/down on module**
J3	17	USB_OTG_TYPEC_SEL	GPIO1_IO09	O	3.3V	**No pull-up/down on module**
J3	21	USB_OTG_SS_RXP	USB2_RX_P	I	3.3V	90Ohm differential pair
J3	23	USB_OTG_SS_RXN	USB2_RX_N	I	3.3V	90Ohm differential pair
J3	27	USB_OTG_SS_TXP	USB2_TX_P	O	3.3V	90Ohm differential pair
J3	29	USB_OTG_SS_TXN	USB2_TX_N	O	3.3V	90Ohm differential pair

Table 3: USB Host & OTG Interface

4.2 SD Card Interface

The PicoCoreMX8MP module can support two SD Card Interfaces (SD_A and SD_B). For specification and licensing please refer the website of the SD Association http://www.sd-card.org.

The SD_A interface can support an external eMMC connection. In this case, SD_A_STROBE pin must be used. For SD Card usage it is recommended to leave this pin open.

The SD_B interface is shared with the WLAN/BT module. This interface is only available, if WLAN/BT isn't mounted on module.

SD_A_VCC is an adjustable voltage supply for SD_A Interface. It can be selected between 3.3V and 1.8V via software adjustment. The current output is limited with 150mA.

SD_B_VCC can be selected between 1.8V and 3.3V via jumpers on module. On a standard configuration (without WLAN/BT), the voltage level of the SD_B signals is 3.3V. Please contact us, if you want to have the 1.8V option.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
SDIO_A						
J2	52	SD_A_VCC		O	1.8V / 3.3V	Selectable; max 150mA output
J2	54	SD_A_STROBE	SD1_STROBE	I	SD_A_VCC	For an external eMMC connec-tion; leave open for SD Card usage
J2	56	SD_A_RST	SD1_RESET_B	O	SD_A_VCC	active low; 100k pull-up on module
J2	58	SD_A_WP	GPIO1_IO07	I	3.3V	
J2	60	SD_A_CD	GPIO1_IO06	I	3.3V	
J2	62	SD_A_CMD	SD1_CMD	O	SD_A_VCC	100k pull-up on module
J2	64	SD_A_CLK	SD1_CLK	O	SD_A_VCC	
J2	66	SD_A_DATA0	SD1_DATA0	I/O	SD_A_VCC	100k pull-up on module
J2	68	SD_A_DATA1	SD1_DATA1	I/O	SD_A_VCC	
J2	70	SD_A_DATA2	SD1_DATA2	I/O	SD_A_VCC	
J2	72	SD_A_DATA3	SD1_DATA3	I/O	SD_A_VCC	
J2	74	SD_A_DATA4	SD1_DATA4	I/O	SD_A_VCC	
J2	76	SD_A_DATA5	SD1_DATA5	I/O	SD_A_VCC	
J2	78	SD_A_DATA6	SD1_DATA6	I/O	SD_A_VCC	
J2	80	SD_A_DATA7	SD1_DATA7	I/O	SD_A_VCC	
SDIO_B [optional with WLAN/BT]						
J2	84	SD_B_RST	SD2_RESET_B	O	SD_B_VCC	active low; 100k pull-up on module
J2	86	SD_B_WP	SD2_WP	I	SD_B_VCC	
J2	88	SD_B_CD	SD2_CD_B	I	SD_B_VCC	
J2	90	SD_B_CMD	SD2_CMD	O	SD_B_VCC	100k pull-up on module
J2	92	SD_B_CLK	SD2_CLK	O	SD_B_VCC	
J2	94	SD_B_DATA0	SD2_DATA0	I/O	SD_B_VCC	100k pull-up on module

J2	96	SD_B_DATA1	SD2_DATA1	I/O	SD_B_VCC	
J2	98	SD_B_DATA2	SD2_DATA2	I/O	SD_B_VCC	
J2	100	SD_B_DATA3	SD2_DATA3	I/O	SD_B_VCC	

Table 4: SD Card Interface Pinout

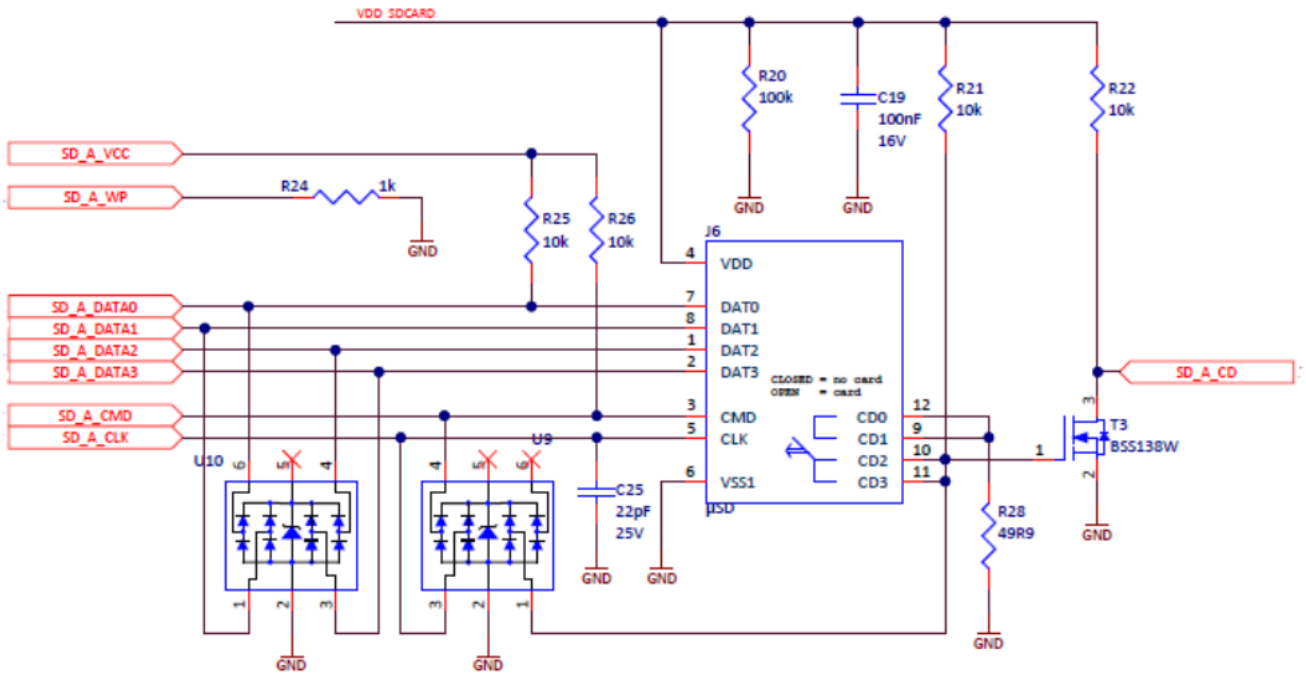

Figure 6: SD Card connector example connection

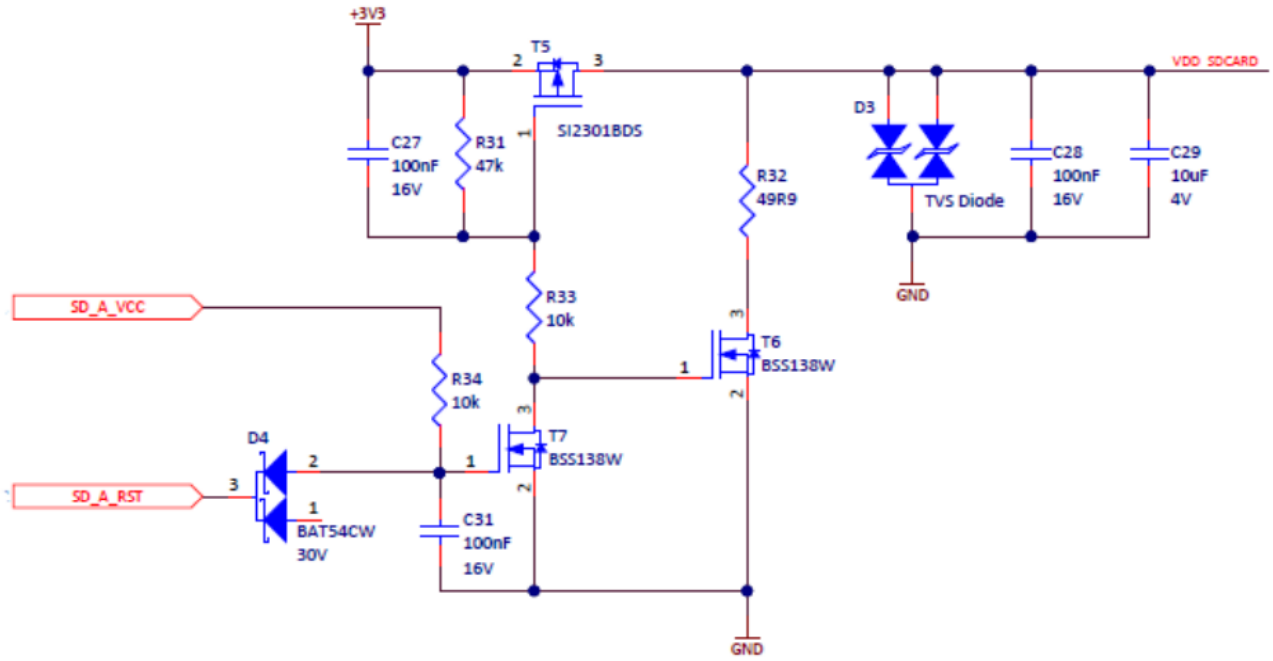

Figure 7: SD_A supply voltage switching circuit

4.3 Serial Peripheral Interface (SPI)

The module support Hi-Speed SPI (Serial Peripheral Interface). All signals are 3.3V compliant. Devices on baseboard with other voltage levels need a level shifter.

Signals don't have pull-ups on module.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	SM*	MM*	Voltage	Remarks
SPI_A							
J1	64	SPI_A_SS0	UART2_TXD	I	O	3.3V	ECSPI3_SS0
J1	66	SPI_A_MISO	UART2_RXD	O	I	3.3V	ECSPI3_MISO
J1	68	SPI_A_MOSI	UART1_TXD	I	O	3.3V	ECSPI3_MOSI
J1	70	SPI_A_SCLK	UART1_RXD	I	O	3.3V	ECSPI3_SCLK
SPI_B							
J1	56	SPI_B_SS0	ECSPI2_SS0	I	O	3.3V	
J1	58	SPI_B_MISO	ECSPI2_MISO	O	I	3.3V	
J1	60	SPI_B_MOSI	ECSPI2_MOSI	I	O	3.3V	
J1	62	SPI_B_SCLK	ECSPI2_SCLK	I	O	3.3V	
SPI_C							
J2	83	SPI_C_SS0	I2C2_SDA	I	O	3.3V	
J2	85	SPI_C_MISO	I2C2_SCL	O	I	3.3V	
J2	87	SPI_C_MOSI	ECSPI1_MOSI	I	O	3.3V	
J2	89	SPI_C_SCLK	ECSPI1_SCLK	I	O	3.3V	

**SM: PicoCoreMX8MP used in Slave Mode, MM: PicoCoreMX8MP used in Slave Mode*

Table 5: Serial Peripheral Interface Pinout

4.4 I2C Interface

The module supports an I2C interface as I2C master. Devices on baseboard with other voltage need a level shifter.

For more chip selects, interrupts and other signals GPIOs can be used and the driver can be modified.

I2C_A signals are shared with CAN_B interface and HDMI GPIOs. For the I2C usage of these signals, it is recommended to place pull-up resistors onto the carrier board (preferably 2.49k or 4.7k)

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
I2C_A						
J1	4	I2C_A_SCL	HDMI_HPD	O	3.3V	**No pull-up/down on module** Optionally: HDMI_CEC Optionally: CAN_B_TX
J1	6	I2C_A_SDA	HDMI_CEC	I/O	3.3V	**No pull-up/down on module** Optionally: HDMI_HPD Optionally: CAN_B_RX
I2C_B						
J1	1	I2C_B_IRQ	GPIO1_IO13	I	3.3V	
J1	3	I2C_B_SCL	I2C4_SCL	O	3.3V	2.49k pull-up on module
J1	5	I2C_B_SDA	I2C4_SDA	I/O	3.3V	2.49k pull-up on module
I2C_C						
J1	40	I2C_C_SCL	ECSPI1_MISO	O	3.3V	2.49k pull-up on module
J1	42	I2C_C_SDA	ECSPI1_SS0	I/O	3.3V	2.49k pull-up on module
I2C_D						
J1	48	I2C_D_SCL	I2C3_SCL	O	3.3V	2.49k pull-up on module
J1	50	I2C_D_SDA	I2C3_SDA	I/O	3.3V	2.49k pull-up on module

Table 6: I2C Interface Pinout

4.5 Serial Interface (UART)

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
UART_A						
J1	14	UART_A_RTS	UART4_RXD	O	3.3V	
J1	16	UART_A_CTS	UART4_TXD	I	3.3V	
J1	18	UART_A_RXD	SAI3_TXFS	I	3.3V	100k pull-up on module
J1	20	UART_A_TXD	SAI3_TXC	O	3.3V	
UART_B						
J1	22	UART_B_RTS	NAND_DATA02	O	3.3V	
J1	24	UART_B_CTS	NAND_DATA03	I	3.3V	
J1	26	UART_B_RXD	NAND_DATA00	I	3.3V	100k pull-up on module
J1	28	UART_B_TXD	NAND_DATA01	O	3.3V	
UART_C						
J1	30	UART_C_RXD	SAI2_RXC	I	3.3V	100k pull-up on module
J1	32	UART_C_TXD	SAI2_RXFS	O	3.3V	
UART_D						
J1	34	UART_D_RXD	UART3_RXD	I	3.3V	100k pull-up on module
J1	36	UART_D_TXD	UART3_TXD	O	3.3V	

Table 7: Serial Interface Pin Out

We recommend to use UART_A for debugging and service only.

F&S standard software uses DCE mode for UART.

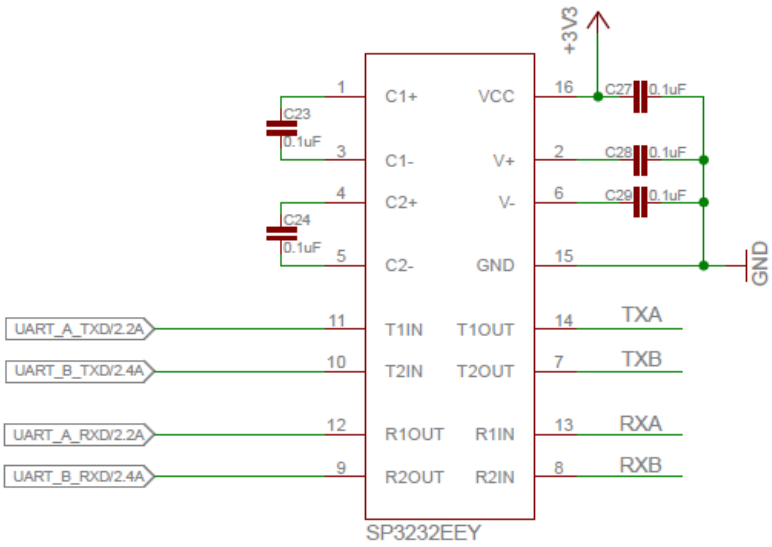

Figure 8: UART transceiver example

4.6 CAN Interface

PicoCoreMX8MP module can support up to 2 CAN buses, which are shared with other interfaces or signals. With the CAN bus usage, the other interfaces cannot be used.

CAN_A interface is shared with HDMI_DDC I2C interface.

CAN_B interface is shared with HDMI_CEC&HDMI_HPD signals and I2C_A interface.

There are no on-module pull-up or pull-downs for the CAN signals.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
CAN_A						
J1	10	CAN_A_RX	HDMI_DDC_SDA	I	3.3V	Optionally: HDMI_DDC_SDA
J1	12	CAN_A_TX	HDMI_DDC_SCL	O	3.3V	Optionally: HDMI_DDC_SCL
CAN_B						
J1	4	CAN_B_TX	HDMI_CEC	O	3.3V	Optionally: HDMI_CEC Optionally: I2C_A_SCL
J1	6	CAN_B_RX	HDMI_HPD	I	3.3V	Optionally: HDMI_HPD Optionally: I2C_A_SDA

Table 8: Serial Interface Pinout

4.7 Ethernet

4.7.1 Ethernet Interface with Gbit PHY

The module supports up to two 10/100/1000 Mbit LAN interfaces via AR8035 Ethernet PHYs.

	Pin	Signal	AR8035 Pad	I/O	Voltage	Remarks
Ethernet A (PHY_1: AR8035)						
J2	1	ETH_A_D1P	TXRXP_A	I/O	1.2V	
J2	3	ETH_A_D1N	TXRXM_A	I/O	1.2V	
J2	5	ETH_A_D2P	TXRXP_B	I/O	1.2V	
J2	7	ETH_A_D2N	TXRXM_B	I/O	1.2V	
J2	9	ETH_A_D3P	TXRXP_C	I/O	1.2V	
J2	11	ETH_A_D3N	TXRXM_C	I/O	1.2V	
J2	13	ETH_A_D4P	TXRXP_D	I/O	1.2V	
J2	15	ETH_A_D4N	TXRXM_D	I/O	1.2V	
J2	17	ETH_A_LED	ACTLED	O	2.5V	Activity LED (RX/TX)
Ethernet B (PHY_2: AR8035) [optional]						
J2	21	ETH_B_LED	ACTLED	O	2.5V	Activity LED (RX/TX)
J2	23	ETH_B_D1P	TXRXP_A	I/O	1.2V	
J2	25	ETH_B_D1N	TXRXM_A	I/O	1.2V	
J2	27	ETH_B_D2P	TXRXP_B	I/O	1.2V	
J2	29	ETH_B_D2N	TXRXM_B	I/O	1.2V	
J2	31	ETH_B_D3P	TXRXP_C	I/O	1.2V	
J2	33	ETH_B_D3N	TXRXM_C	I/O	1.2V	
J2	35	ETH_B_D4P	TXRXP_D	I/O	1.2V	
J2	37	ETH_B_D4N	TXRXM_D	I/O	1.2V	

Table 9: Ethernet A & B Signals

4.7.2 Ethernet RGMII Interface

Without Ethernet PHYs: The module supports one 10/100/1000Mbit LAN interface via RGMII signals. The RGMII signals can be reached from the B2B Connector.

An external Ethernet-PHY or an external Ethernet switch is required on baseboard/carrier board.

Over the ETH_A_LED, ETH_B_LED, ETH_B_D4P and ETH_B_D4N there are 4 GPIOs that can be either used for the external switch or PHY (i.e. Reset, Interrupt, Enable etc.).

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
RGMII Interface [optional]						
J2	1	ETH_A_D1P	ENET _MDC	O	1.8V	
J2	3	ETH_A_D1N	ENET_MDIO	I/O	1.8V	
J2	5	ETH_A_D2P	ENET_TX_CTL	O	1.8V	
J2	7	ETH_A_D2N	ENET_TXC	O	1.8V	
J2	9	ETH_A_D3P	ENET_TD0	O	1.8V	
J2	11	ETH_A_D3N	ENET_TD1	O	1.8V	
J2	13	ETH_A_D4P	ENET_ TD2	O	1.8V	
J2	15	ETH_A_D4N	ENET_ TD3	O	1.8V	
J2	17	ETH_A_LED	SAI3_RXFS	O	3.3V	Standard GPIO
J2	21	ETH_B_LED	SAI3_RXC	O	3.3V	Standard GPIO
J2	23	ETH_B_D1P	ENET_RX_CTL	I	1.8V	
J2	25	ETH_B_D1N	ENET_RXC	I	1.8V	
J2	27	ETH_B_D2P	ENET_RD0	I	1.8V	
J2	29	ETH_B_D2N	ENET_RD1	I	1.8V	
J2	31	ETH_B_D3P	ENET_ RD2	I	1.8V	
J2	33	ETH_B_D3N	ENET_ RD3	I	1.8V	
J2	35	ETH_B_D4P	GPIO1_IO11	O	3.3V	Standard GPIO
J2	37	ETH_B_D4N	GPIO1_IO04	O	3.3V	Standard GPIO

Table 10: RGMII Interface Signals

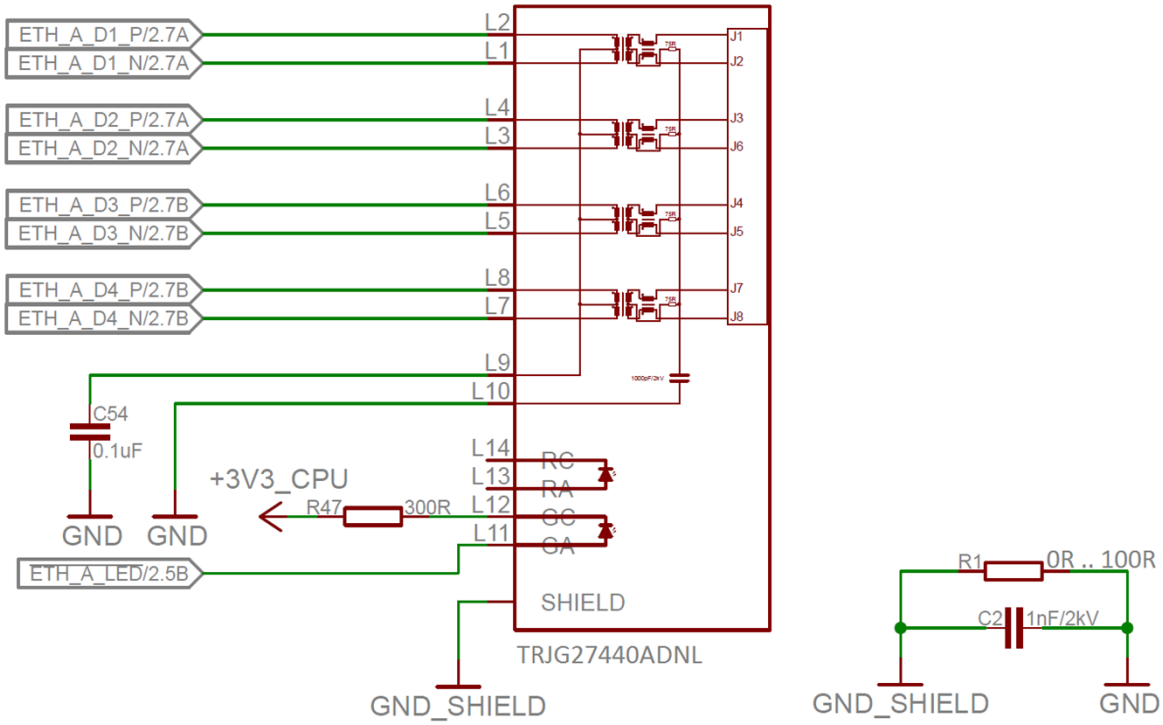

Figure 9: LAN output example

4.8 Audio

The PicoCoreMX8MP module can support audio interface either directly via I2S signals or with an external audio codec IC. The audio codec NXP SGTL5000 can be mounted on the module optionally. In this case the module can also support the MIC function.

AUDIO_A_VCC is supplied from the PMIC on PicoCore Module as default. For a better and smoother audio quality an external low-noise power supply (e.g. LDO) is highly recommended (3V~3.3V – 5mA). In this case, the intern voltage source must be separated from the audio circuitry. Please contact us to have the correct jumper configuration for the external-supplied AUDIO_A_VCC.

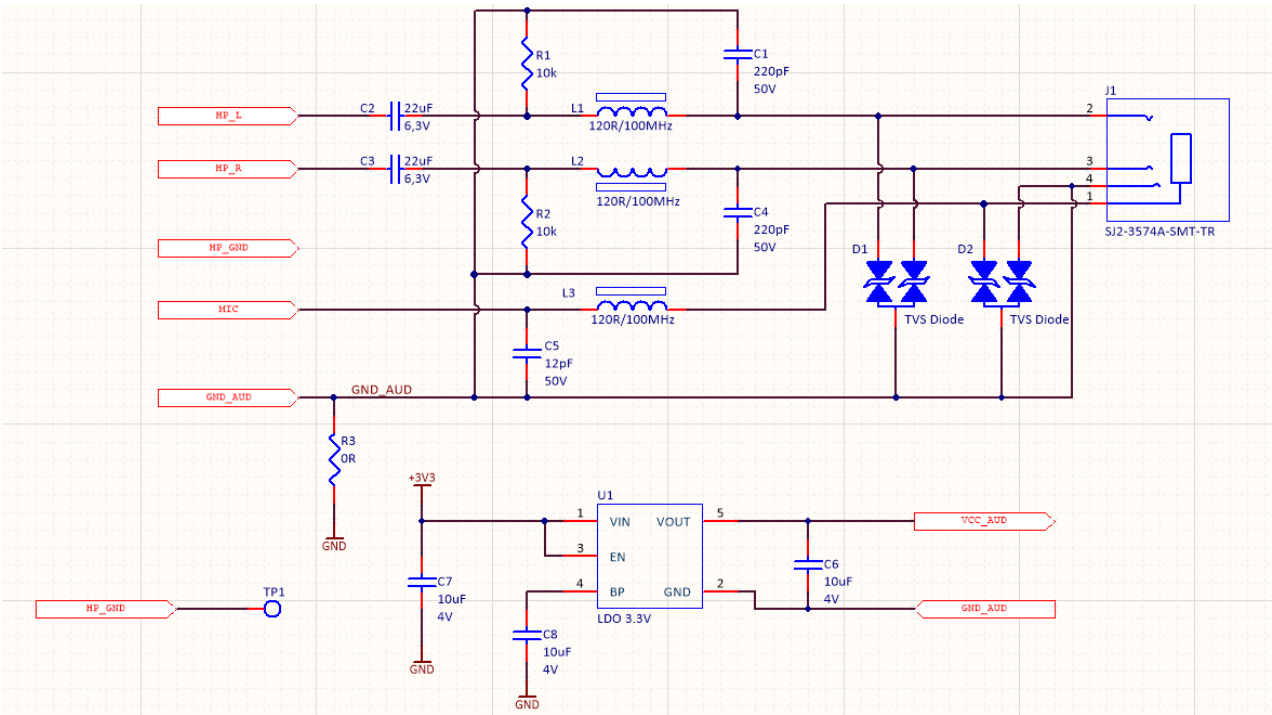

Figure 10: Headphone-Out Mic-In Example Circuit

	Pin	Signal	CPU Pad	I/O	Voltage*	Remarks
Audio A – with Audio Codec (SGTL5000) [optional]						
J2	2	AUDIO_A_VCC	VDDA	PWR	3V/3.3V	max 16.50mW power consumption
J2	4	AUDIO_A_GND	AGND	PWR	GND	
J2	6	AUDIO_A_LOUT_L	LOUT	O	3V/3.3V	
J2	8	AUDIO_A_LOUT_R	ROUT	O	3V/3.3V	
J2	10	AUDIO_A_MIC	MICIN	I	3V/3.3V	
J2	12	AUDIO_A_LIN_L	LLINEIN	I	3V/3.3V	
J2	14	AUDIO_A_LIN_R	RLINEIN	I	3V/3.3V	
J2	18	AUDIO_A_HP_L	LHPOUT	O	3V/3.3V	
J2	20	AUDIO_A_HP_R	RHPOUT	O	3V/3.3V	
J2	22	AUDIO_A_HP_GND	HP_VGND	O	GND	
Audio A – I2S Option (without Audio Codec) [standard]						
J2	2	AUDIO_A_VCC	N.C.	-	-	Do Not Connect! Leave open
J2	4	AUDIO_A_GND	N.C.	-	-	Do Not Connect! Leave open
J2	6	AUDIO_A_LOUT_L	SAI2_TXC	I/O	3.3V	I2S_A_TXC
J2	8	AUDIO_A_LOUT_R	SAI2_TXFS	I/O	3.3V	I2S_A_TXFS
J2	10	AUDIO_A_MIC	N.C.	-	-	Do Not Connect! Leave open
J2	12	AUDIO_A_LIN_L	SAI2_MCLK	O	3.3V	I2S_A_MCLK
J2	14	AUDIO_A_LIN_R	N.C.	-	-	Do Not Connect! Leave open
J2	18	AUDIO_A_HP_L	SAI2_RXD0	I	3.3V	I2S_A_RXD
J2	20	AUDIO_A_HP_R	SAI2_TXD0	O	3.3V	I2S_A_TXD
J2	22	AUDIO_A_HP_GND	N.C.	-	-	Do Not Connect! Leave open

**Depends on the AUDIO_A_VCC source*

Table 11: Audio A Interface

Audio B can used in 3 different ways. These ways are shown in the table below.

“No function” describes that the pin has no functionality with that specific usage. Those pins are also connected to a CPU pin and can be used as GPIOs. Please be careful that these signals have 1.8V voltage level.

	Pin	Signal	CPU Pad	I/O	Voltage	Function
Audio B – 3-Channel Input (option1)						
J2	65	AUDIO_B_I2S_MCLK	SAI1_MCLK	O	1.8V	SAI5_MCLK
J2	67	AUDIO_B_I2S_TXFS	SAI5_TXFS	I	1.8V	SAI5_RXD1
J2	69	AUDIO_B_I2S_TXC	SAI5_TXC	I	1.8V	SAI5_RXD2
J2	73	AUDIO_B_I2S_TXD	SAI5_TXD0	I	1.8V	SAI5_RXD3
J2	75	AUDIO_B_I2S_RXD	SAI1_RXD0	X	X	No function (can be used as GPIO)
J2	77	AUDIO_B_I2S_RXFS	SAI5_RXFS	I/O	1.8V	SAI5_RXFS
J2	79	AUDIO_B_I2S_RXC	SAI5_RXC	I/O	1.8V	SAI5_RXC
Audio B – 1 Channel Output (option2)						
J2	65	AUDIO_B_I2S_MCLK	SAI1_MCLK	O	1.8V	SAI5_MCLK
J2	67	AUDIO_B_I2S_TXFS	SAI5_TXFS	I/O	1.8V	SAI5_TXFS
J2	69	AUDIO_B_I2S_TXC	SAI5_TXC	I/O	1.8V	SAI5_TXC
J2	73	AUDIO_B_I2S_TXD	SAI5_TXD0	O	1.8V	SAI5_TXD0
J2	75	AUDIO_B_I2S_RXD	SAI1_RXD0	X	X	No function (can be used as GPIO)
J2	77	AUDIO_B_I2S_RXFS	SAI5_RXFS	X	X	No function (can be used as GPIO)
J2	79	AUDIO_B_I2S_RXC	SAI5_RXC	X	X	No function (can be used as GPIO)
Audio B – Symmetrical Codec [1-2x LINE-IN or Microphone & 1x LINE-OUT or Headphone] (option3)						
J2	65	AUDIO_B_I2S_MCLK	SAI1_MCLK	O	1.8V	SAI5_MCLK
J2	67	AUDIO_B_I2S_TXFS	SAI5_TXFS	I	1.8V	SAI5_RXD1
J2	69	AUDIO_B_I2S_TXC	SAI5_TXC	I	1.8V	SAI5_RXD2
J2	73	AUDIO_B_I2S_TXD	SAI5_TXD0	O	1.8V	SAI5_TXD0
J2	75	AUDIO_B_I2S_RXD	SAI1_RXD0	X	X	No function (can be used as GPIO)
J2	77	AUDIO_B_I2S_RXFS	SAI5_RXFS	I/O	1.8V	SAI5_RXFS
J2	79	AUDIO_B_I2S_RXC	SAI5_RXC	I/O	1.8V	SAI5_RXC

Table 12: Audio B Interface

4.9 PCIE Interface

The PicoCoreMX8MP module supports single lane PCI Express Gen 2. The interface can work as root complex or endpoint (Dual mode operation).

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
PCIe Interface						
J1	77	mPCIE_CTX_P	PCIE_TXN_P	O	1.8V	
J1	79	mPCIE_CTX_N	PCIE_TXN_N	O	1.8V	
J1	83	mPCIE_CRX_P	PCIE_RXN_P	I	1.8V	
J1	85	mPCIE_CRX_N	PCIE_RXN_N	I	1.8V	
J1	89	mPCIE_CLK_P	PCIE_REF_PAD_CLK_P	O	1.8V	
J1	91	mPCIE_CLK_N	PCIE_REF_PAD_CLK_N	O	1.8V	
J1	95	mPCIE_PERST	SAI3_RXD	O	3.3V	mPCIe power reset; no pull-up/-down on module
J1	97	mPCIE_WAKE	SAI3_TXD	I	3.3V	mPCIe wakeup; no pull-up/-down on module

Table 13: PCIE Interface

4.10 Display Interface

The PicoCoreMX8MP module can support MIPI DSI interface, HDMI 2.0a, and LVDS interface. As long as no more than two interfaces are in use simultaneously, up to 1080p60 is supported.

On the module there are 2 display channels. Display interfaces can be reached via those channels optionally. The possible display combinations are:

Configuration	Channel A	Channel B
DSI + HDMI	4-lane MIPI-DSI	HDMI 2.0a
DSI + LVDS	4-lane MIPI-DSI	4-lane LVDS
LVDS + HDMI	4-lane LVDS	HDMI 2.0a
LVDS + LVDS	8-lane LVDS	

Table 14: Display Combinations

4.10.1 Display Channel A (MIPI-DSI or LVDS)

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
Channel A – MIPI-DSI Configuration						
J1	17	DSI_A_CLK_P	MIPI_DSI1_CLK_P	O	1.8V	
J1	19	DSI_A_CLK_N	MIPI_DSI1_CLK_N	O	1.8V	
J1	23	DSI_A_DATA0_P	MIPI_DSI1_D0_P	O	1.8V	
J1	25	DSI_A_DATA0_N	MIPI_DSI1_D0_N	O	1.8V	
J1	29	DSI_A_DATA1_P	MIPI_DSI1_D1_P	O	1.8V	
J1	31	DSI_A_DATA1_N	MIPI_DSI1_D1_ N	O	1.8V	
J1	35	DSI_A_DATA2_P	MIPI_DSI1_D2_ P	O	1.8V	
J1	37	DSI_A_DATA2_N	MIPI_DSI1_D2_ N	O	1.8V	
J1	41	DSI_A_DATA3_P	MIPI_DSI1_D3_ P	O	1.8V	
J1	43	DSI_A_DATA3_N	MIPI_DSI1_D3_ N	O	1.8V	
Channel A – LVDS Configuration						
J1	17	DSI_A_CLK_P	LVDS0_CLK_P	O	1.8V	
J1	19	DSI_A_CLK_N	LVDS0_CLK_N	O	1.8V	
J1	23	DSI_A_DATA0_P	LVDS0_D0_P	O	1.8V	
J1	25	DSI_A_DATA0_N	LVDS0_D0_N	O	1.8V	
J1	29	DSI_A_DATA1_P	LVDS0_D1_P	O	1.8V	
J1	31	DSI_A_DATA1_N	LVDS0_D1_N	O	1.8V	
J1	35	DSI_A_DATA2_P	LVDS0_D2_P	O	1.8V	
J1	37	DSI_A_DATA2_N	LVDS0_D2_N	O	1.8V	
J1	41	DSI_A_DATA3_P	LVDS0_D3_P	O	1.8V	
J1	43	DSI_A_DATA3_N	LVDS0_D3_N	O	1.8V	

Table 15: MIPI DSI / LVDS Interface

4.10.2 Display Channel B (HDMI or LVDS)

The module supports quad lane MIPI CSI interface.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
Channel B – HDMI Configuration						
J1	47	DSI_B_CLK_P	HDMI_TXC_P	O	1.8V	
J1	49	DSI_B_CLK_N	HDMI_TXC_N	O	1.8V	
J1	53	DSI_B_DATA0_P	HDMI_TX0_P	O	1.8V	
J1	55	DSI_B_DATA0_N	HDMI_TX0_N	O	1.8V	
J1	59	DSI_B_DATA1_P	HDMI_TX1_P	O	1.8V	
J1	61	DSI_B_DATA1_N	HDMI_TX1_N	O	1.8V	
J1	65	DSI_B_DATA2_P	HDMI_TX2_P	O	1.8V	
J1	67	DSI_B_DATA2_N	HDMI_TX2_N	O	1.8V	
J1	71	DSI_B_DATA3_P	EARC_N_HPD	O	1.8V	
J1	73	DSI_B_DATA3_N	EARC_P_UTIL	O	1.8V	
J1	4	HDMI_CEC	HDMI_CEC	O	3.3V	optionally: CAN_B_TX optionally: I2C_A_SCL
J1	6	HDMI_HPD	HDMI_HPD	I	3.3V	optionally: CAN_B_RX optionally: I2C_A_SDA
J1	10	HDMI_DDC_SDA	HDMI_DDC_SDA	I/O	3.3V	2.49k pull-up on module optionally: CAN_A_RX
J1	12	HDMI_DDC_SCL	HDMI_DDC_SCL	O	3.3V	2.49k pull-up on module optionally: CAN_A_TX
Channel B – LVDS Configuration						
J1	47	DSI_B_CLK_P	LVDS1_CLK_P	O	1.8V	
J1	49	DSI_B_CLK_N	LVDS1_CLK_N	O	1.8V	
J1	53	DSI_B_DATA0_P	LVDS1_D0_P	O	1.8V	
J1	55	DSI_B_DATA0_N	LVDS1_D0_N	O	1.8V	
J1	59	DSI_B_DATA1_P	LVDS1_D1_P	O	1.8V	
J1	61	DSI_B_DATA1_N	LVDS1_D1_N	O	1.8V	
J1	65	DSI_B_DATA2_P	LVDS1_D2_P	O	1.8V	
J1	67	DSI_B_DATA2_N	LVDS1_D2_N	O	1.8V	
J1	71	DSI_B_DATA3_P	LVDS1_D3_P	O	1.8V	
J1	73	DSI_B_DATA3_N	LVDS1_D3_N	O	1.8V	

Table 16: MIPI DSI / LVDS Interface

4.11 Camera Serial Interface (MIPI-CSI)

The module supports up to 2 quad-lane MIPI-CSI interfaces.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
MIPI-CSI Channel A						
J1	74	CSI_A_CLK_P	MIPI_CSI1_CLK_P	I	1.8V	
J1	76	CSI_A_CLK_N	MIPI_CSI1_CLK_N	I	1.8V	
J1	80	CSI_A_DATA0_P	MIPI_CSI1_D0_P	I	1.8V	
J1	82	CSI_A_DATA0_N	MIPI_CSI1_D0_N	I	1.8V	
J1	86	CSI_A_DATA1_ P	MIPI_CSI1_D1_P	I	1.8V	
J1	88	CSI_A_DATA1_ N	MIPI_CSI1_D1_N	I	1.8V	
J1	92	CSI_A_DATA2_ P	MIPI_CSI1_D2_P	I	1.8V	
J1	94	CSI_A_DATA2_ N	MIPI_CSI1_D2_N	I	1.8V	
J1	98	CSI_A_DATA3_ P	MIPI_CSI1_D3_P	I	1.8V	
J1	100	CSI_A_DATA3_ N	MIPI_CSI1_D3_N	I	1.8V	
MIPI-CSI Channel B [optional]						
J3	4	CSI_B_CLK_P	MIPI_CSI2_CLK_P	I	1.8V	
J3	6	CSI_B_CLK_N	MIPI_CSI2_CLK_N	I	1.8V	
J3	10	CSI_B_DATA0_P	MIPI_CSI2_D0_P	I	1.8V	
J3	12	CSI_B_DATA0_N	MIPI_CSI2_D0_N	I	1.8V	
J3	16	CSI_B_DATA1_ P	MIPI_CSI2_D1_P	I	1.8V	
J3	18	CSI_B_DATA1_ N	MIPI_CSI2_D1_N	I	1.8V	
J3	22	CSI_B_DATA2_ P	MIPI_CSI2_D2_P	I	1.8V	
J3	24	CSI_B_DATA2_ N	MIPI_CSI2_D2_N	I	1.8V	
J3	28	CSI_B_DATA3_ P	MIPI_CSI2_D3_P	I	1.8V	
J3	30	CSI_B_DATA3_ N	MIPI_CSI2_D3_N	I	1.8V	

Table 17: MIPI CSI Interface

4.12 WLAN and Bluetooth Interface

The PicoCore™MX8MP contains a certified high performance WLAN and Bluetooth module.

The module is based on NXP W8997 chip, having CE, FCC, IC, NCC, AU/NZ, India, Japan certificates. Please contact support@fs-net.de for additional information about process of certification.

The module offers:

- IEEE802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, Bluetooth 3.0 and Bluetooth 5.0 (supports low Energy)

Information about Bluetooth (QDID):

Please refer to the following BT QDID info for 88W8997 (AW-CM276NF).

QDID: D046929

https://launchstudio.bluetooth.com/ListingDetails/91724

If Bluez-5.37 will be used, the QDID from NXP can be used

https://launchstudio.bluetooth.com/ListingDetails/92249

Customer can use this QDIDs to create their device QDID.

Note: In case WLAN/BT module is mounted only one external SD card interface (SD_A) is available and SD_B is not available.

4.13 GPIO

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pull-up's or pull-down's are configurable by software, but they are not available at board start-up. On a non-powered board it's not allowed to have a voltage on GPIO pins. Also a higher voltage as the announced IO power is not allowed.

	Pin	Standard	CPU Pad	Voltage	Remarks
J1	2	GPIO_J1_2	GPIO1_IO15	3.3V	
J1	7	GPIO_J1_7	SPDIF_EXT_CLK	3.3V	Can also PWM
J1	44	GPIO_J1_44	NAND_ALE	3.3V	
J1	46	GPIO_J1_46	NAND_CE0_B	3.3V	
J1	52	GPIO_J1_52	NAND_DQS	3.3V	
J1	54	GPIO_J1_54	GPIO1_IO01	3.3V	Can also PWM
J2	63	PWM	GPIO1_IO10	3.3V	PWM Output (PWM3)

Table 18: JTAG Interface

For the alternative usages of all Pins please refer to GPIO Reference Card.

4.14 JTAG

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	93	JTAG_TCK	JTAG_TCK*1	I	1.8V	Test Clock
J2	95	JTAG_TMS	JTAG_TMS*1	I	1.8V	Test Mode Select
J2	97	JTAG_TDI	JTAG_TDI*1	I	1.8V	Test Data In
J2	99	JTAG_TDO	JTAG_TDO*1	O	1.8V	Test Data Out

Table 19: JTAG Interface

- For debug only
- Leave unconnected, if you don't use JTAG
- Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU

4.15 Power and Power Control Pins

	Pin	Signal	I/O	Description
J2	24 26 28	VDD_VIN	I	Main Power supply input please refer chapter 8 Electrical characteristic
J2	30 32 34	GND[*5]	I	Main Power supply Ground input
J2	36	VDD_VBAT[*1]	I	RTC battery input; tie to 3.0V please refer chapter 8 Electrical characteristic
J2	40	VDD_3V.3[*2]	O	20mA output from on module DCDC powered from VDD_VIN
J2	52	SD_A_VCC	I	SDHC power output; 3.3V or 1.8V; max 150mA
J2	51	USB_OTG_VBUS	I	USB Phy voltage input; 5V
J2	41	USB_HOST_VBUS	I	USB Phy voltage input; 5V
J2	42	RESETIN[*3]	I	Power on reset input; 100k Pull-Up to 1.8V
J2	44	PMIC_STBY[*4]	O	Active high for going to SUSPEND state
J2	46	PMIC_ON_REQ	O	Active high for going to RUN state
J2	48	ON_OFF	I	CPU On/Off control pin, can be used with an external button
J2	2	AUDIO_A_VCC	I	External supply for audio codec; 3~3.3V – 5mA

Table 20: Power and Power Control

[*1] By using a battery for VBAT the regulation rules have to be followed. Please check with your test laboratory. It's possible to use a supercap instead.

[*2] VDD_3V3 is the 3.3V @20mA power supply of the module generated from PMIC and powered from VDD_VIN. Can be used as an "Enable Signal" for the power regulators on baseboard. Please do not use VDD_3V3 pin as a power supply for carrier board.

[*3] RESETINN is a Reset Input for the module. Will just reset the CPU. Button or an Open Collector/Open Drain output will restart the CPU. On power fail VDD_VIN has to be switched off and on to avoid latch up effects.

[*4] PMIC_STBY is going to high, if the CPU is going in standby. This allows switch of peripheral functions and save more power. Wakeup needs support by the driver, you have to check.

[*5] The GND contacts which are given in the table above are the power ground contacts for VDD_VIN. For a better EMC performance it is highly recommended to connect all GND contacts to GND on the carrier board (not just the power ground contacts).

4.16 Boot Mode

	Pin	Signal	I/O	Description
J2	50	BOOTSEL	I	Boot Mode selection

Table 21: Boot Mode

The PicoCore™MX8MP boots from eMMC (determined by fuse).

If booting from eMMC is not possible due to a corrupted bootloader, the PicoCore™MX8MP can be placed in recovery mode with the BOOTSEL signal.

Leave the pin open for normal boot.

Pull the pin to GND with 0R for recovery mode.

You need a special tool to write the bootloader to the board.

You can download the recovery tool from www.fs-net.de

5 Flash

5.1 eMMC Flash

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

The PicoCoreMX8MP module can support up to 32GB eMMC flash memory.

6 Real Time Clock (RTC)

There is a NXP PCF85263ATL or a compatible RTC component implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

7 Secure Authenticator IC

The secure tamper-resistant authentication IC NXP EdgeLock™ SE050 offers a strong cryptographic solution intended to be used by device manufacturers to prove the authenticity of their genuine products. It can be used for brand protection, revenue protection, and or customer safety.

For more information visit NXPs website.

This component is optional and not mounted in all configurations. Please contact sales to get more information.

8 Electrical characteristic

8.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IO pins	-0.3	OVDD+0.3	V
Input Voltage range 1.8V IO pins	-0.3	2.15	V
Voltage on any IO with VIN off		0.3	V
USB_*_VBUS	-0.3	5.6	V
Maximum power consumption VDD_VBAT at 85°C		0.6	µA
Maximum output current 3.3V		20	mA

Table 22: Absolute Maximum Ratings

8.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Max	Unit
+5VS	Module main power		4.5	5.5	V
VDD_VBAT	RTC power		0.9	5.5	V
USB_*_VBUS	USB supply voltage		4.5	5.5	
OVDD	On module 3.3V DCDC		3.15	3.45	V
VDD_3V3	3.3V output for power enable on carrier board		OVDD	OVDD	V
V_{ih}	High Level Input Voltage		0.7*OVDD	OVDD	V
V_{il}	Low Level Input Voltage		0	0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15		V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA		0.15	V
I_o	Output current IOs	3.3V		5	mA

Table 23: DC Electrical Characteristics

9 Thermal Specification

This Embedded Module is a high-performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors (housing, power consumption, heat spreader, airflow and many others).

In order to keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
- For reducing the heat dissipation, CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS) as well as “Thermal throttling”, by an integrated temperature sensor.
    - The integrated sensor measures the die-temperature and lowers CPU clock or shut down CPU if needed.
    - DVFS lowers CPU clock and core voltage in accordance with the performance needed from the application.

For optimal use of DVFS, modify your software to only use peak performance only for short times.

The housing has big influence on the heat dissipation. There are many points to analyze:

- Is there the option of dissipating heat to the housing?
- Is there a possibility that the air can circulate in the housing?
- Is an active cooling possible?

The surrounding heat has a big effect to the temperature of the system.

Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction!

The following table shows nominal thermal specification of the module:

Description	Min	Typ.	Max	Unit
Consumer Range Environmental Temperature	0		+70	°C
Consumer Range CPU Junction Temperature	0		+95	°C
Industrial Range Environmental Temperature (I)	-20		+85	°C
Industrial Range CPU Junction Temperature (I)	-40		+105	°C
Extended Industrial Range Environmental Temperature (XI)	-40		+85	°C
Extended Industrial Range CPU Junction Temperature (XI)	-40		+105	°C
Junction to Package Top **(Ψ_{JT})**		0.98		°C/W

Table 24: Thermal Specs

Note 1: Maximum junction temperature of the CPU is 95°C /105°C. Cooling is necessary and highly recommended for operations near the limits. See also: Power Consumption and Power Consumption and Cooling

Please get in contact with F&S for recommended cooling solutions.

Note 2: WLAN/BT is -30°C to +85°C only. This component is not critical for the booting operation.

Note 3: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN13273 (https://www.nxp.com/docs/en/application-note/AN13273.pdf)

10 Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

11 ESD and EMC Implementing

Like all other COM modules on the market there is no ESD protection on any signal out from the COM module. ESD protection has to be placed as near as possible to the ESD source - this is the connector with external access on the COM baseboard.

A helpful guide is available from TI: ESD Protection Layout Guide

The module supports spread spectrum in order to reduce the electromagnetic interference (EMI). This will normally reduce the EMI between 9 and 12 dB and so this can decrease your shielding requirements. We highly recommend to have controlled impedances and wires as short as possible in your layout designs.

12 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

13 Power Consumption and Cooling

Depending on your product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

For the optimal cooling performance we recommend to use F&S heat spreader set MHS.PC100.1. For more information please contact with us.

14 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months

Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months

For longer storage we recommend vacuum dry packs.

15 ROHS and REACH Statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.

Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.

Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

16 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags. The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

17 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 11: Matrix Code Sticker

18 Appendix

Important Notice

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