Hardware Documentation

PicoCore™MX8MM /MX8MN for HW Revision 1.30 PicoCore™MX8MMr2 /MX8MNr2*

**LPDDR4 Version*

Version 016
(2024-05-22)

Elektronik Systeme

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About This Document

This document describes how to use the PicoCore™MX8MM/MN(r2) boards with mechanical and electrical information. The latest version of this document can be found at:

https://www.fsembedded.com.

This document is written for the PicoCoreMX8MM / MX8MN modules, which have LP-DDR4 DRAM and optional WLAN/BT connectivity. The related standard boards are given in the table below.

The PCB Name of the LPDDR4 Version is: PicoCoreMX8MM (latest HW Version 1.30)

Important Note!

The latest PCB version for PicoCore™MX8MM/MN is Version 1.30, for PicoCore™MX8MM/MN r2 is Version 1.00.

The only difference between these two modules is their Gbit Ethernet PHY's.

PicoCore™MX8MM/MN → Qualcomm Atheros AR8035

PicoCore™MX8MMr2/MNr2 → Realtek RTL8211F/D

Related Modules
PicoCore™MX8MM-V1-LIN – i.MX8M Mini Processor based
PicoCore™MX8MM-V2-LIN – i.MX8M Mini Processor based
PicoCore™MX8MM-V3-LIN – i.MX8M Mini Processor based
PicoCore™MX8MM-V4-LIN – i.MX8M Mini Processor based
PicoCore™MX8MMr2-V1-LIN – i.MX8M Mini Processor based
PicoCore™MX8MMr2-V2-LIN – i.MX8M Mini Processor based
PicoCore™MX8MMr2-V3-LIN – i.MX8M Mini Processor based
PicoCore™MX8MMr2-V4-LIN – i.MX8M Mini Processor based

Attention: Please also note the circuit diagram of our Baseboard reference design. https://fs-net.de/assets/download/docu/PicoCore/PicoCoreBBDSI_eng.pdf

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
24.09.2019	001	All		-	Initial Version	MW
21.11.2019	002	All	M	3.1, 4.4	Minor Changings	MD
19.02.2020	003	All	M	3.1	Minor Changings	MD
27.05.2020	004	All	A	2	Addition of contact 1 marker for the J1 and J2 connectors	MD
13.07.2020	005	All	M	3.1, 4, 4.7	Correction of functions and voltage levels, correction for UART_RTS and CTS contacts	MD
14.09.2020	006	All	M	4, 4.2, 4.9	Update of the example circuit diagrams, extra information for SD_A_VSEL and VCC_AUD contacts	MD
09.10.2020	007	All	M M	5 11	Information to the contact VDD_3V3 & VDD_SNVS Updates on thermal specifications	MD
04.05.2021	008	All	A.M	All	New HW Version (1.30) – New Functionalities: CAN FD, RGMII Interface, Dual Channel LVDS, QSPI Support	MD
23.06.2021	009	All	M	3.1, 4	Correction on the CPU Pads of some GPIOs	MD
21.07.2021	010	All	M A	- All	Changing the name of the document PicoCoreMX8MN support is added	MD
29.07.2021	011	All	M	4.13	Updated information about network controller	JK
02.11.2021	012	All	M	11, 15	Thermal specifications are updated	MD
12.01.2022	013	All	A, M	4.6	Change Naming of Table 8	MW
17.05.2023	014	All	A	6	Add description for boot mode and pin BOOTSEL	HF
29.04.2024	015	All	M	4.1	Correct description of USB_H1_VBUS	MW
14.05.2024	016	All	M	4.15	Correct / add information for PWM functionality	TM

V	Version
A,M,R	Added, Modified, Removed
Au	Author

Table of Contents

1 Block diagram

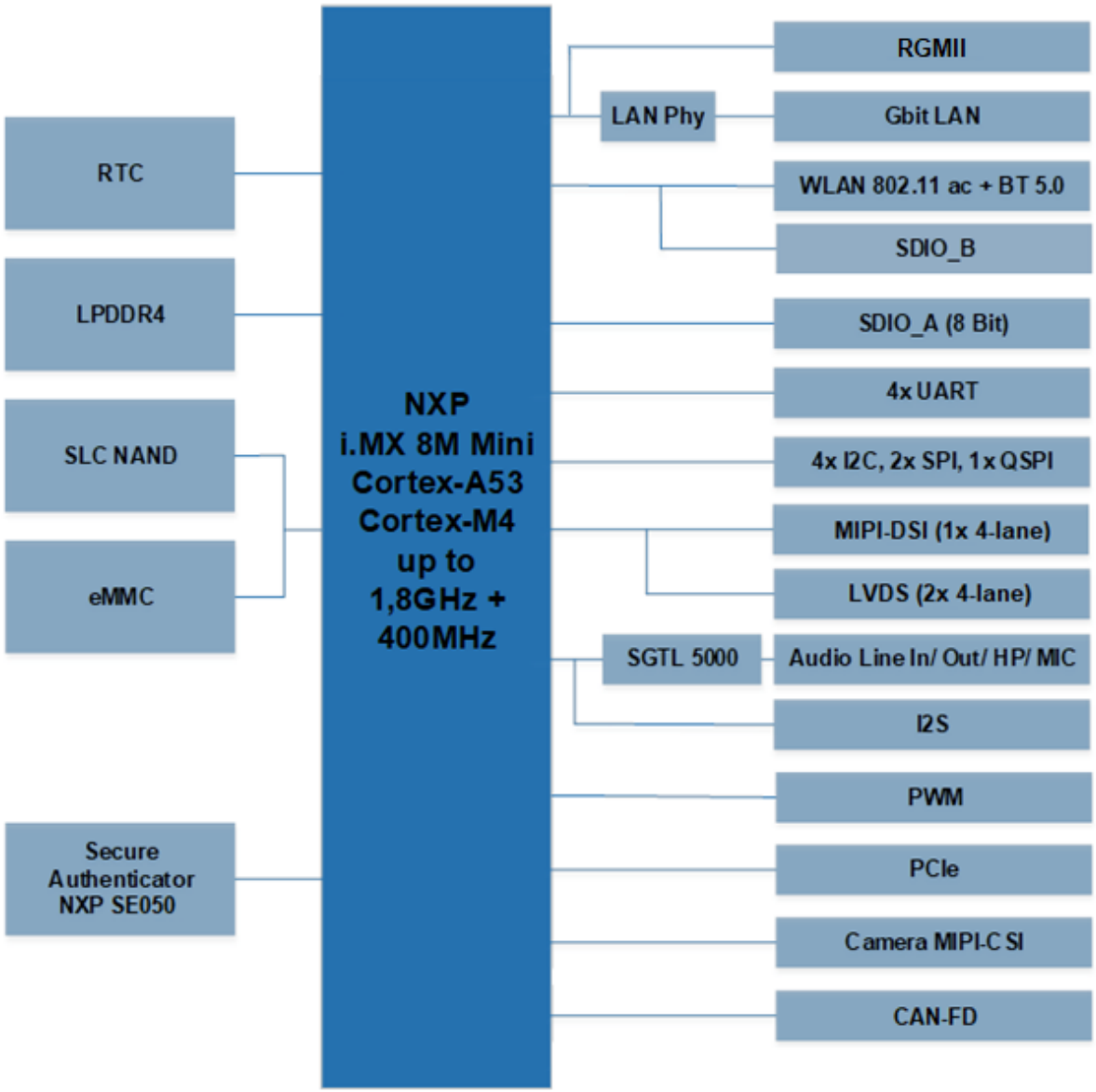

Figure 1: Block Diagram

2 Mechanical Dimension

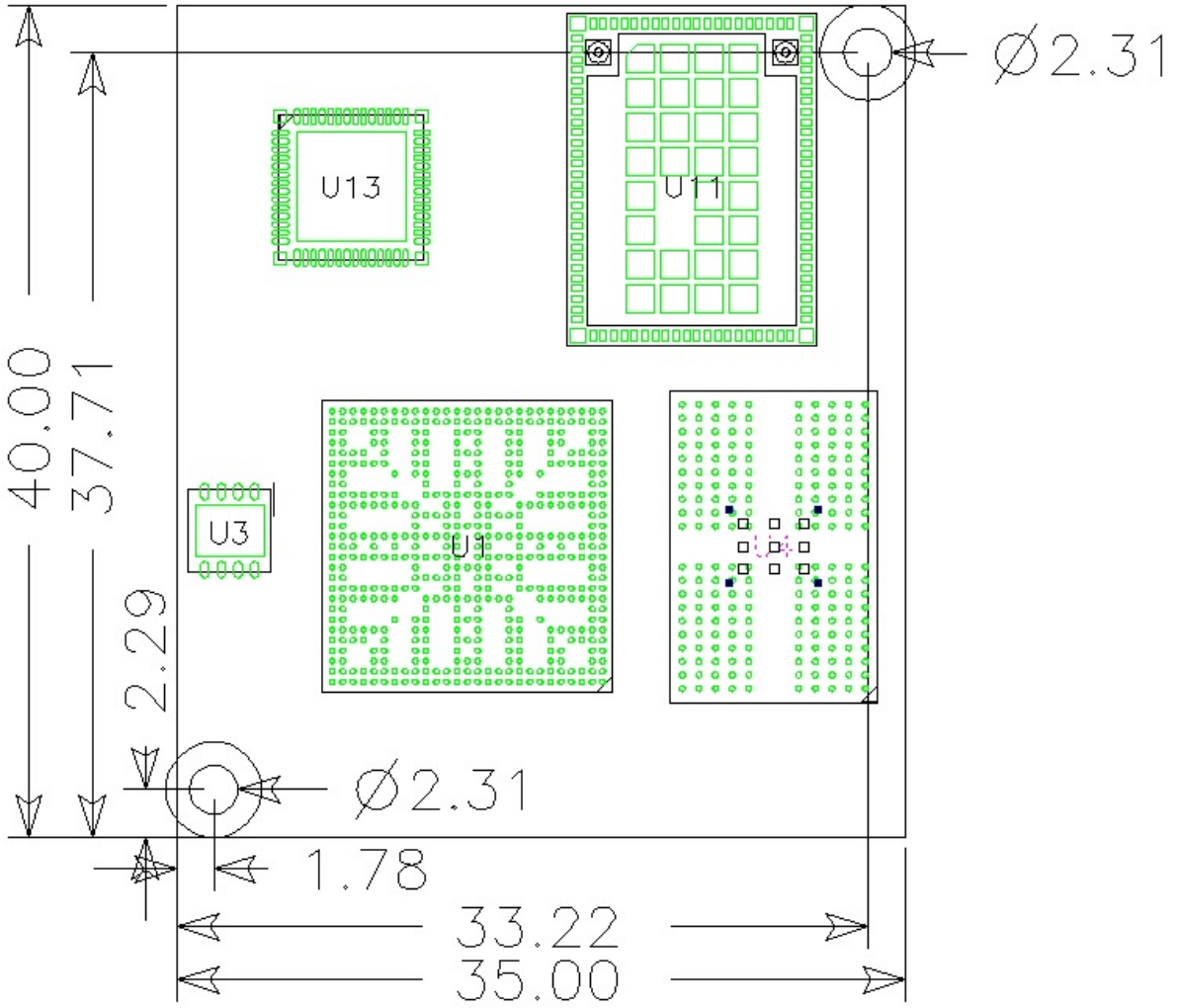

Figure 2: Mechanical Dimension Top

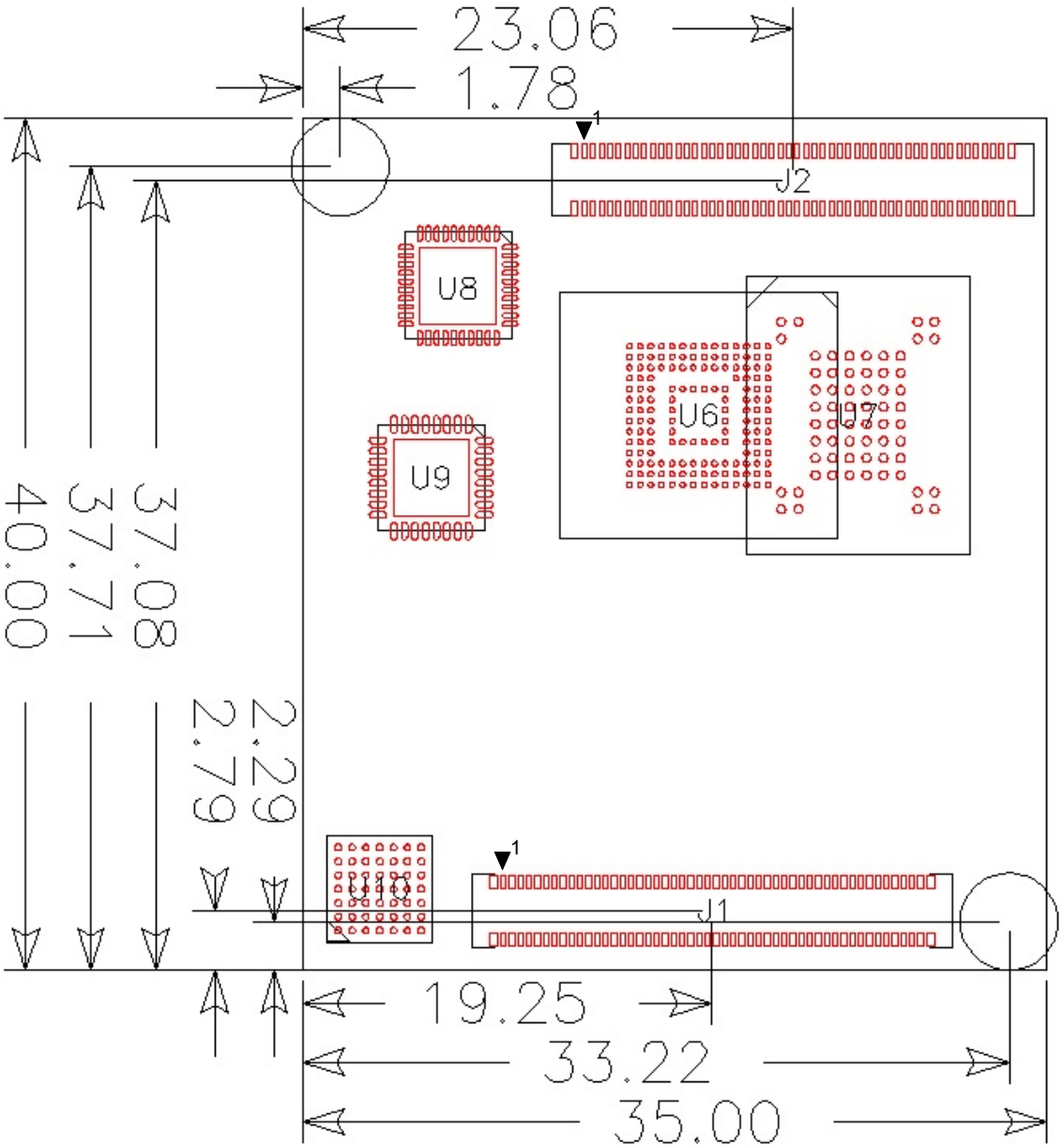

Figure 3: Mechanical Dimension Bottom

Dimensions	Description
Size	40mm x 35mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	Max. 5mm
Height of the parts on the bottom side	Max. 1.4mm
Weight	14gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

2.1 SMT Steel Spacer

For mounting we recommend SMT Steel Spacer components, order number **B.MSCHR.22**. This part is in F&S stock and can be ordered via F&S web shop.

The stack height of the space is 1.5mm. If a different stack height is needed, another spacer should be chosen.

Data sheet and 3D model (STP) is available on our website.

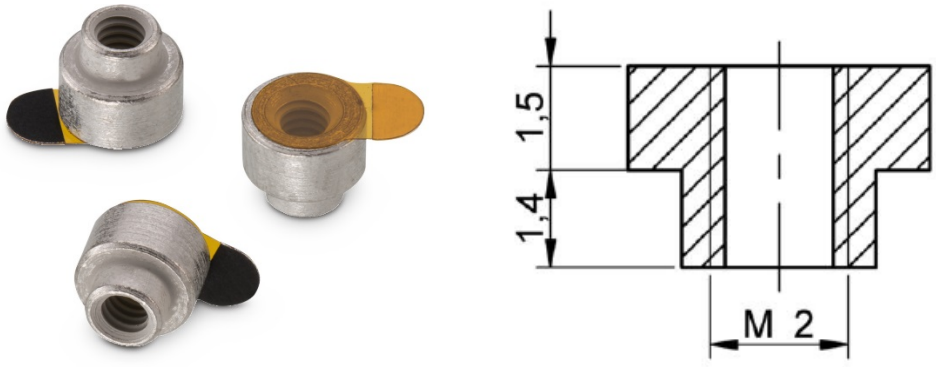

Figure 4: WE SMT Steel Spacer

2.2 Heat Spreader

As a base for the cooling concept, F&S offers a heat spreader. Part number of heat spreader is **MHS.PC100.1** and can be ordered via F&S web shop.

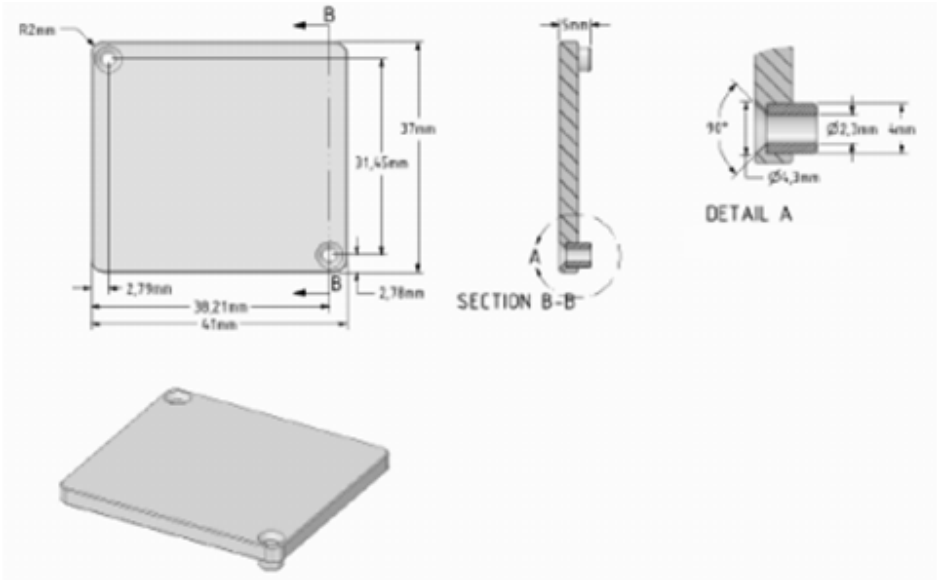

Figure 5: Heat Spreader (Images are not to scale)

3 Interface and Signal Description

3.1 B2B Connectors

PicoCoreMX8MM/MN modules have two 100 contacts connectors from manufacturer Hirose.

Part number: DF40C-100DP-0.4V

Part number counterpart: DF40C-100DS-0.4V

With this combination you get the minimal stacking height of 1,5mm. Another possible stacking height by using different counterpart connector is: 3mm. The connector with 1,5mm stacking height is available at F&S and can be ordered via web shop.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	1	I2C_B_IRQ	GPIO1_IO00	I	3.3V	
J1	2	GPIO_J1_2	GPIO1_IO13	I/O	3.3V	Standard GPIO
J1	3	I2C_B_SCL	I2C2_SCL	O	3.3V	
J1	4	I2C_A_SCL	I2C1_SCL	O	3.3V	
J1	5	I2C_B_SDA	I2C2_SDA	I/O	3.3V	
J1	6	I2C_A_SDA	I2C1_SDA	I/O	3.3V	
J1	7	GPIO_J1_7	GPIO1_IO01	I/O	3.3V	
J1	8	GND		PWR	GND	
J1	9	BL_ON	SPDIF_TX	O	3.3V	
J1	10	CAN_RX		I	3.3V	*1
J1	11	BL_PWM	SPDIF_RX	O	3.3V	
J1	12	CAN_TX		O	3.3V	*1
J1	13	VLCD_ON	SAI3_RXFS	O	3.3V	
J1	14	UART_A_RTS	SAI2_TXFS	O	3.3V	
J1	15	GND		PWR	GND	
J1	16	UART_A_CTS	SAI2_RXD0	I	3.3V	
J1	17	DSI_A_CLK_P	MIPI_DSI_CLK_P	O	1.2V/200mV	*2 MIPI-DSI/LVDS_A
J1	18	UART_A_RXD	UART1_RXD	I	3.3V	
J1	19	DSI_A_CLK_N	MIPI_DSI_CLK_N	O	1.2V/200mV	*2 MIPI-DSI/LVDS_A
J1	20	UART_A_TXD	UART1_TXD	O	3.3V	
J1	21	GND		PWR	GND	
J1	22	UART_B_RTS	SAI3_RXC	O	3.3V	
J1	23	DSI_A_DATA0_P	MIPI_DSI_D0_P	O	1.2V/200mV	*2 MIPI-DSI/LVDS_A
J1	24	UART_B_CTS	SAI3_RXD	I	3.3V	
J1	25	DSI_A_DATA0_N	MIPI_DSI_D0_N	O	1.2V/200mV	*2 MIPI-DSI/LVDS_A
J1	26	UART_B_RXD	UART2_RXD	I	3.3V	
J1	27	GND		PWR	GND	

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	28	UART_B_TXD	UART2_TXD	O	3.3V	
J1	29	DSI_A_DATA1_P	MIPI_DSI_D1_P	O	1.2V/200mV	*2 MIPI-DSI/LVDS_A
J1	30	UART_C_RXD	UART4_RXD	I	3.3V	
J1	31	DSI_A_DATA1_N	MIPI_DSI_D1_N	O	1.2V/200mV	*2 MIPI-DSI/LVDS_A
J1	32	UART_C_TXD	UART4_TXD	O	3.3V	
J1	33	GND		PWR	GND	
J1	34	UART_D_RXD	UART3_RXD	I	3.3V	
J1	35	DSI_A_DATA2_P	MIPI_DSI_D2_P	O	1.2V/200mV	*2 MIPI-DSI/LVDS_A
J1	36	UART_D_TXD	UART3_TXD	O	3.3V	
J1	37	DSI_A_DATA2_N	MIPI_DSI_D2_N	O	1.2V/200mV	*2 MIPI-DSI/LVDS_A
J1	38	GND		PWR	GND	
J1	39	GND		PWR	GND	
J1	40	I2C_C_SCL	I2C3_SCL	O	3.3V	
J1	41	DSI_A_DATA3_P	MIPI_DSI_D3_P	O	1.2V/200mV	*2 MIPI-DSI/LVDS
J1	42	I2C_C_SDA	I2C3_SDA	I/O	3.3V	
J1	43	DSI_A_DATA3_N	MIPI_DSI_D3_N	O	1.2V/200mV	*2 MIPI-DSI/LVDS
J1	44	GPIO_J1_44	GPIO1_IO08	I/O	3.3V	
J1	45	GND		PWR	GND	
J1	46	GPIO_J1_46	GPIO1_IO09	I/O	3.3V	
J1	47	DSI_B_CLK_P		O	1.2V/200mV	*3 LVDS_B
J1	48	I2C_D_SCL	I2C4_SCL	O	3.3V	Shared I2C
J1	49	DSI_B_CLK_N		O	1.2V/200mV	*3 LVDS_B
J1	50	I2C_D_SDA	I2C4_SDA	I/O	3.3V	Shared I2C
J1	51	GND		PWR	GND	
J1	52	GPIO_J1_52	GPIO1_IO10	I/O	3.3V	
J1	53	DSI_B_DATA0_P		O	1.2V/200mV	*3 LVDS_B
J1	54	GPIO_J1_54	GPIO1_IO11	I/O	3.3V	
J1	55	DSI_B_DATA0_N		O	1.2V/200mV	*3 LVDS_B
J1	56	SPI_B_SS0	ECSPI2_SS0	I/O	3.3V	
J1	57	GND		PWR	GND	
J1	58	SPI_B_MISO	ECSPI2_MISO	I/O	3.3V	
J1	59	DSI_B_DATA1_P		O	1.2V/200mV	*3 LVDS_B
J1	60	SPI_B_MOSI	ECSPI2_MOSI	I/O	3.3V	
J1	61	DSI_B_DATA1_N		O	1.2V/200mV	*3 LVDS_B
J1	62	SPI_B_SCLK	ECSPI2_SCLK	I/O	3.3V	
J1	63	GND		PWR	GND	
J1	64	SPI_A_SS0	ECSPI1_SS0	I/O	3.3V	
J1	65	DSI_B_DATA2_P		O	1.2V/200mV	*3 LVDS_B

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	66	SPI_A_MISO	ECSPI1_MISO	I/O	3.3V	
J1	67	DSI_B_DATA2_N		O	1.2V/200mV	*3 LVDS_B
J1	68	SPI_A_MOSI	ECSPI1_MOSI	I/O	3.3V	
J1	69	GND		PWR	GND	
J1	70	SPI_A_SCLK	ECSPI1_SCLK	I/O	3.3V	
J1	71	DSI_B_DATA3_P		O	1.2V/200mV	*3 LVDS_B
J1	72	GND		PWR	GND	
J1	73	DSI_B_DATA3_N		O	1.2V/200mV	*3 LVDS_B
J1	74	CSI_CLK_P	MIPI_CSI_CLK_P	I	1.8V	
J1	75	GND		PWR	GND	
J1	76	CSI_CLK_N	MIPI_CSI_CLK_N	I	1.8V	
J1	77	MPCIE_CTX_P	PCIE_TXN_P	O		
J1	78	GND		PWR	GND	
J1	79	MPCIE_CTX_N	PCIE_TXN_N	O		
J1	80	CSI_DATA0_P	MIPI_CSI_D0_P	I	1.8V	
J1	81	GND		PWR	GND	
J1	82	CSI_DATA0_N	MIPI_CSI_D0_N	O	1.8V	
J1	83	MPCIE_CRX_P	PCIE_RXN_P	I		
J1	84	GND		PWR	GND	
J1	85	MPCIE_CRX_N	PCIE_RXN_N	I		
J1	86	CSI_DATA1_P	MIPI_CSI_D1_P	I	1.8V	
J1	87	GND		PWR	GND	
J1	88	CSI_DATA1_N	MIPI_CSI_D1_N	I	1.8V	
J1	89	MPCIE_CLK_P	PCIE_CLK_P	O		
J1	90	GND		PWR	GND	
J1	91	MPCIE_CLK_N	PCIE_CLK_N	O		
J1	92	CSI_DATA2_P	MIPI_CSI_D2_P	I	1.8V	
J1	93	GND		PWR	GND	
J1	94	CSI_DATA2_N	MIPI_CSI_D2_N	I	1.8V	
J1	95	MPCIE_PERST	SAI5_RXFS	O	3.3V	
J1	96	GND		PWR	GND	
J1	97	MPCIE_WAKE	SAI5_RXC	I	3.3V	
J1	98	CSI_DATA3_P	MIPI_CSI_D3_P	I	1.8V	
J1	99	GND		PWR	GND	
J1	100	CSI_DATA3_N	MIPI_CSI_D3_N	I	1.8V	

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	1	ETH_A_D1P		I/O		1 channel ETH PHY 1Gbit
J2	2	AUDIO_A_VCC		I	3V	*4 Optional
J2	3	ETH_A_D1N		I/O		1 channel ETH PHY 1Gbit
J2	4	AUDIO_A_GND		I	GND	*4 Optional
J2	5	ETH_A_D2P		I/O		1 channel ETH PHY 1Gbit
J2	6	AUDIO_A_LOUT_L		O		*4 Line-Out left
J2	7	ETH_A_D2N		I/O		1 channel ETH PHY 1Gbit
J2	8	AUDIO_A_LOUT_R		O		*4 Line-Out right
J2	9	ETH_A_D3P		I/O		1 channel ETH PHY 1Gbit
J2	10	AUDIO_A_MIC		I		Microphone-In
J2	11	ETH_A_D3N		I/O		1 channel ETH PHY 1Gbit
J2	12	AUDIO_A_LIN_L		I		*4 Line-In left
J2	13	ETH_A_D4P		I/O		1 channel ETH PHY 1Gbit
J2	14	AUDIO_A_LIN_R		I		Line-In right
J2	15	ETH_A_D4N		I/O		1 channel ETH PHY 1Gbit
J2	16	GND		PWR	GND	
J2	17	ETH_A_LED		O		Eth PHY Activity LED
J2	18	AUDIO_A_HP_L		O		*4 Headphone left
J2	19	GND		PWR	GND	
J2	20	AUDIO_A_HP_R		O		*4 Headphone right
J2	21	ETH_B_LED	N.C.	O		No support
J2	22	AUDIO_A_HP_GND		O		*4 Never connect to GND!
J2	23	ETH_B_D1P	N.C.			No support
J2	24	VDD_VIN		PWR	5.0V	*5 Supply voltage input
J2	25	ETH_B_D1N	N.C.			No support
J2	26	VDD_VIN		PWR	5.0V	*5 Supply voltage input
J2	27	ETH_B_D2P	N.C.			No support
J2	28	VDD_VIN		PWR	5.0V	*5 Supply voltage input
J2	29	ETH_B_D2N	N.C.			No support
J2	30	GND		PWR	GND	
J2	31	ETH_B_D3P	N.C.			No support
J2	32	GND		PWR	GND	
J2	33	ETH_B_D3N	N.C.			No support
J2	34	GND		PWR	GND	
J2	35	ETH_B_D4P	N.C.			No support
J2	36	VDD_VBAT		PWR	0.9V ~ 5.5V	*5 RTC battery input
J2	37	ETH_B_D4N	N.C.			No support

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	38	VDD_SNVS		I	2.7V-5.0V	*5 SNVS voltage input
J2	39	GND		PWR	GND	
J2	40	VDD_3V3		O	3.3V	*5 3.3V @20mA output
J2	41	USB_HOST_VBUS	USB2_VBUS	I	5.0V	*5
J2	42	RESETINN	PWRON	I	1.8V (3.3V - Rev1.00)	*5 Power on reset input; onboard pull-up 10k
J2	43	USB_HOST_DP	USB2_DP	I/O		
J2	44	PMIC_STBY	PMIC_STBY_REQ	O	1.8V	*5
J2	45	USB_HOST_DN	USB2_DN	I/O		
J2	46	PMIC_ON_REQ	PMIC_ON_REQ	O	1.8V	*5
J2	47	USB_HOST_PWRN	GPIO1_IO14	O	3.3V	
J2	48	ON_OFF		I	1.8V	*5 On/Off input for CPU
J2	49	GND		PWR	GND	
J2	50	BOOTSEL		I	1.8V	Service jumper; normally left open; ee Chapter 6 Boot Mode
J2	51	USB_OTG_VBUS	USB1_VBUS	I	5.0V	USB Phy voltage supply
J2	52	SD_A_VCC		O	1.8V / 3.3V	Selectable
J2	53	USB_OTG_PWRN	GPIO1_IO12	O	3.3V	
J2	54	RESERVED	---			RESERVED
J2	55	USB_OTG_ID	USB1_ID	I	3.3V	Input
J2	56	SD_A_RST	SD1_RESET_B	O	3.3V	
J2	57	USB_OTG_DP	USB1_DP	I/O		
J2	58	SD_A_WP	GPIO1_IO07	I	3.3V	
J2	59	USB_OTG_DN	USB1_DN	I/O		
J2	60	SD_A_CD	GPIO1_IO06	I	3.3V	
J2	61	GND		PWR	GND	
J2	62	SD_A_CMD	SD1_CMD	I/O	SD_A_VCC	
J2	63	PWM	SPDIF_EXT_CLK	O	3.3V	
J2	64	SD_A_CLK	SD1_CLK	O	SD_A_VCC	
J2	65	GPIO_J2_65	SAI1_TXD7	I/O	3.3V	*6
J2	66	SD_A_DATA0	SD1_DATA0	I/O	SD_A_VCC	onboard pull-up 100k
J2	67	GPIO_J2_67	SAI1_TXD6	I/O	3.3V	*6
J2	68	SD_A_DATA1	SD1_DATA1	I/O	SD_A_VCC	
J2	69	GPIO_J2_69	SAI1_TXD4	I/O	3.3V	*6
J2	70	SD_A_DATA2	SD1_DATA2	I/O	SD_A_VCC	
J2	71	GND		PWR	GND	
J2	72	SD_A_DATA3	SD1_DATA3	I/O	SD_A_VCC	

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	73	GPIO_J2_73	SAI1_TXD5	I/O	3.3V	*6
J2	74	SD_A_DATA4	SD1_DATA4	I/O	SD_A_VCC	
J2	75	GPIO_J2_75	SAI1_RXD5	I/O	3.3V	*6
J2	76	SD_A_DATA5	SD1_DATA5	I/O	SD_A_VCC	
J2	77	GPIO_J2_77	SAI1_RXD6	I/O	3.3V	*6
J2	78	SD_A_DATA6	SD1_DATA6	I/O	SD_A_VCC	
J2	79	GPIO_J2_79	SAI1_RXD4	I/O	3.3V	*6
J2	80	SD_A_DATA7	SD1_DATA7	I/O	SD_A_VCC	
J2	81	GND		PWR	GND	
J2	82	GND		PWR	GND	
J2	83	GPIO_J2_83	SAI1_MCLK	O	3.3V	*6
J2	84	SD_B_RST	SD2_RST	O	SD_B_VCC	*7
J2	85	GPIO_J2_85	SAI1_RXD7	I	3.3V	*6
J2	86	SD_B_WP	SD2_WP	I	SD_B_VCC	*7
J2	87	GPIO_J2_87	SAI1_TXC	O	3.3V	*6
J2	88	SD_B_CD	SD2_CD_B	I	SD_B_VCC	*7
J2	89	GPIO_J2_89	SAI1_RXD0	O	3.3V	*6
J2	90	SD_B_CMD	SD2_CMD	I/O	SD_B_VCC	*7
J2	91	GND		PWR	GND	
J2	92	SD_B_CLK	SD2_CLK	O	SD_B_VCC	*7
J2	93	JTAG_TCK	JTAG_TCK	I	1.8V	
J2	94	SD_B_DATA0	SD2_DATA0	I/O	SD_B_VCC	*7
J2	95	JTAG_TMS	JTAG_TMS	I	1.8V	
J2	96	SD_B_DATA1	SD2_DATA1	I/O	SD_B_VCC	*7
J2	97	JTAG_TDI	JTAG_TDI	I	1.8V	
J2	98	SD_B_DATA2	SD2_DATA2	I/O	SD_B_VCC	*7
J2	99	JTAG_TDO	JTAG_TDO	O	1.8V	
J2	100	SD_B_DATA3	SD2_DATA3	I/O	SD_B_VCC	*7

Table 2: B2B connector

*1: The older HW Versions (until 1.30) do not support the CAN-Interface. These contacts have no connections.

*2: These contacts have optional connections/features. See Chapter 4.12 for the connections.

*3: With the HW Version 1.30 the module can support two 4-Lane LVDS Interface (Older HW Versions have just one display channel and the pins of the second LVDS Channel should be left open).

*4: These contacts have optional connections/features. See Chapter 4.10 for the connections.

*5: Please see Chapter 4.17 for further information about these power & control contacts.

*6: These contacts have optional connections/features. See Chapter 4.16 for the connections.

*7: These contacts have optional connections/features. See Chapter 4.4 for the connections.

4 Interfaces

4.1 USB OTG & Host

PicoCoreMX8MM/MN modules can support 1x USB HOST Mode and 1x USB OTG.

The 90 Ohm differential pair of USB signals doesn't need any termination. For external ports ESD and EMV protection is required nearby the USB connector.

If the USB OTG will be used in Host Mode, contact **USB_OTG_ID** must be connected to GND via a resistor. Otherwise it must be directly connected to the USB connector.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	41	USB_H1_VBUS*[1]	USB2_VBUS	I	5.0V	Input; USB Phy voltage supply*[3]
J2	45	USB_H1_DN*[1]	USB2_DN	I/O		90 Ohm differential pair; Preferred for host
J2	43	USB_H1_DP*[1]	USB2_DP	I/O		
J2	47	USB_H1_PWRn*[1]*[2]	GPIO1_IO14	O	3.3V	Power enable; onboard Pull-Up 100k
J2	51	USB_OTG_VBUS	USB1_VBUS	I	5.0V	Input; USB Phy voltage supply
J2	53	USB_OTG_PWRn	GPIO1_IO12	O	3.3V	onboard Pull-Up 10k
J2	55	USB_OTG_ID	USB1_ID	I	3.3V	Input
J2	57	USB_OTG_DP	USB1_DP	I/O		90 Ohm differential pair
J2	59	USB_OTG_DN	USB1_DN	I/O		

Table 3: USB Host Interface

*[1] **PicoCoreMX8MN** modules only have one USB OTG. And the related pins (J2_41, J2_43, J2_45) on the connector are N.C. (USB Host option is not supported.)

*[2] USB_HOST_PWRn pin can be used as a standard GPIO on the modules that have i.MX8M Nano processor.

*[3] Also connect 5V if used as USB Host

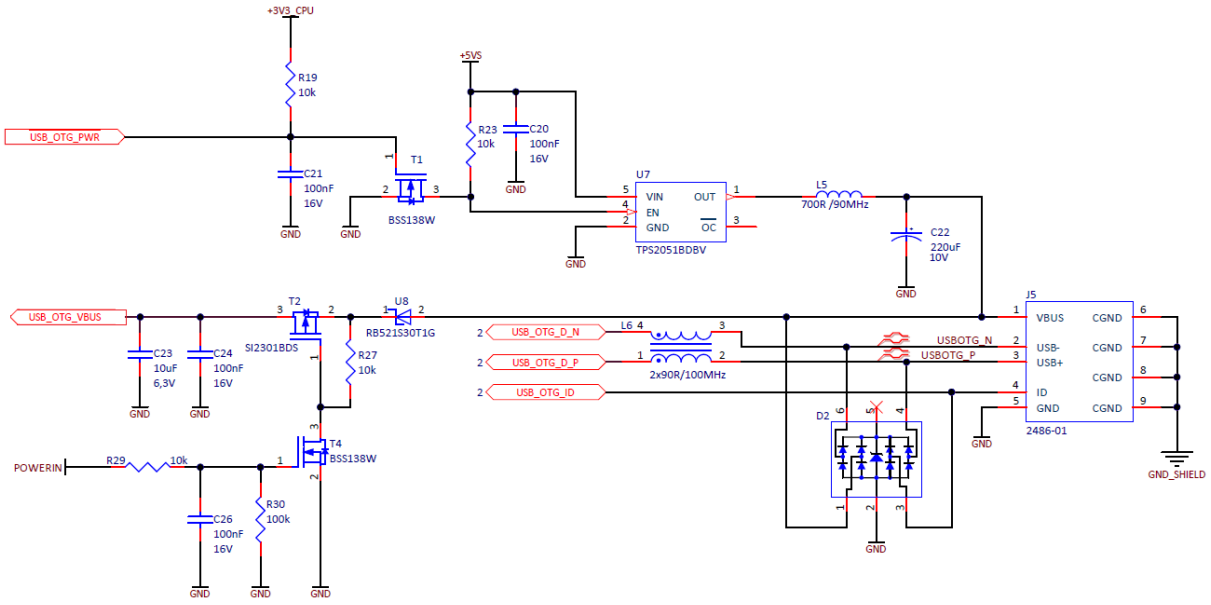

Figure 6: USB OTG example connection

4.2 SD Card Interface A

This interface is supporting a SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

SD_A_VCC can be 1.8V or as 3.3V. The voltage level is configured by the driver.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	52	SD_A_VCC	NVCC_SD1	O	1.8V / 3.3V	Power supply out for external SDIO interface
J2	54	RESERVED	RESERVED	N/A	N/A	*1Do not connect. Reserved for future use.
J2	56	SD_A_RST	SD1_RESET_B	O	SD_A_VCC	
J2	58	SD_A_WP	GPIO1_IO07	I	3.3V	Active low write protect disable
J2	60	SD_A_CD	GPIO1_IO06	I	3.3V	Active low card detect
J2	62	SD_A_CMD	SD1_CMD	I/O	SD_A_VCC	Command/Response, onboard pull-up 100k
J2	64	SD_A_CLK	SD1_CLK	O	SD_A_VCC	
J2	66	SD_A_DATA0	SD1_DATA0	I/O	SD_A_VCC	onboard pull-up 100k
J2	68	SD_A_DATA1	SD1_DATA1	I/O	SD_A_VCC	
J2	70	SD_A_DATA2	SD1_DATA2	I/O	SD_A_VCC	
J2	72	SD_A_DATA3	SD1_DATA3	I/O	SD_A_VCC	
J2	74	SD_A_DATA4	SD1_DATA4	I/O	SD_A_VCC	
J2	76	SD_A_DATA5	SD1_DATA5	I/O	SD_A_VCC	
J2	78	SD_A_DATA6	SD1_DATA6	I/O	SD_A_VCC	
J2	80	SD_A_DATA7	SD1_DATA7	I/O	SD_A_VCC	

Table 4: SD Card Interface A

*1: In previous versions of the documentation this contact was described as SD_A_VSEL. This was not correct.

4.3 SD Card Interface B

This interface is supporting a SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

This SD card Interface is shared with the WLAN/BT module. The Interface is only available if WLAN/BT module isn't mounted.

The supply voltage of SD_B (SD_B_VCC) can be set to 1.8V or 3.3V via mounting option.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	84	SD_B_RST	SD2_RESET_B	O	SD_B_VCC	onboard pull-up 100k
J2	86	SD_B_WP	SD2_WP	I	SD_B_VCC	Active low write protect disable
J2	88	SD_B_CD	SD2_CD_B	I	SD_B_VCC	Active low card detect
J2	90	SD_B_CMD	SD2_CMD	I/O	SD_B_VCC	Command/Response, onboard pull-up 100k
J2	92	SD_B_CLK	SD2_CLK	O	SD_B_VCC	
J2	94	SD_B_DATA0	SD2_DATA0	I/O	SD_B_VCC	onboard pull-up 100k
J2	96	SD_B_DATA1	SD2_DATA1	I/O	SD_B_VCC	
J2	98	SD_B_DATA2	SD2_DATA2	I/O	SD_B_VCC	
J2	100	SD_B_DATA3	SD2_DATA3	I/O	SD_B_VCC	

Table 5: SD Card Interface B

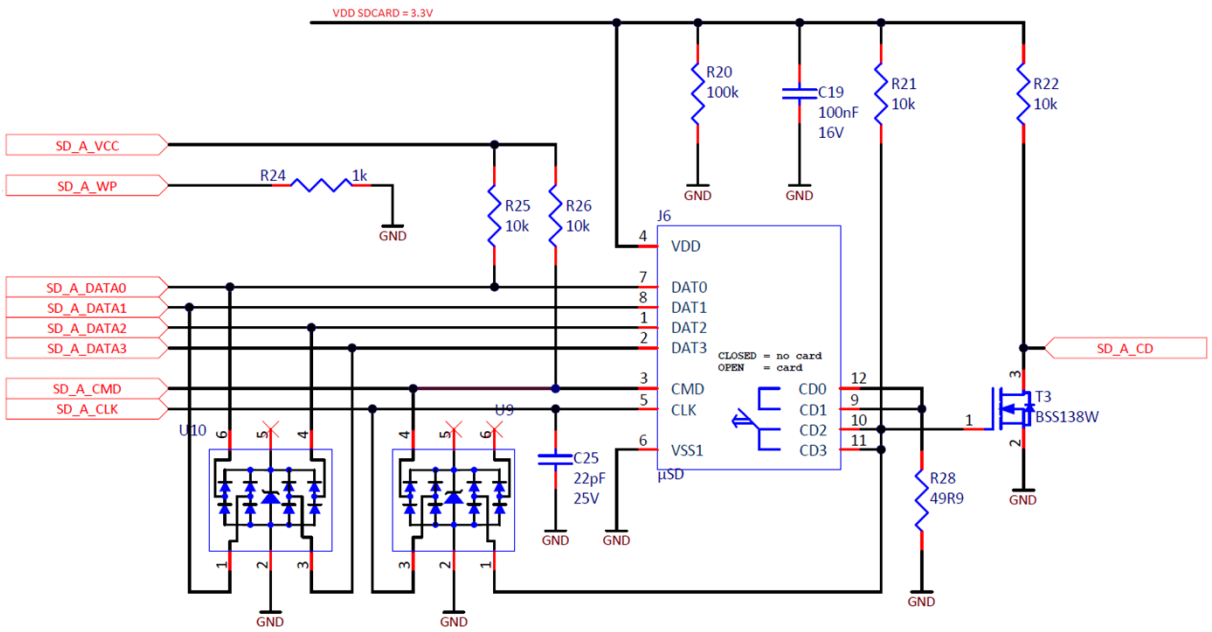

Figure 7: SD Card connector example connection

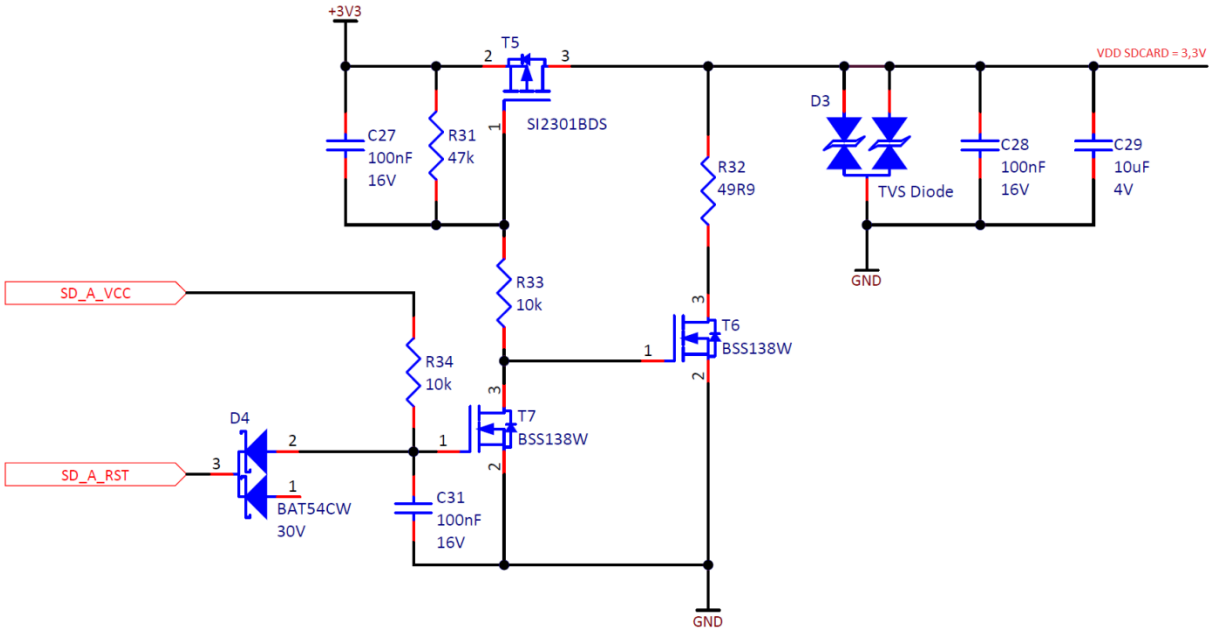

Figure 8: SD_A supply voltage switching circuit

4.4 SPI

The module support HS SPI (Serial Peripheral Interface). All signals are 3.3V compliant. Devices on baseboard with other voltage need a level shifter.

Signals don't have pull-ups on module.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	SM*2	MM*2	Voltage	Description
J1	64	SPI_A_SS0	ECSPI1_SS0	I	O	3.3V	
J1	66	SPI_A_MISO	ECSPI1_MISO	O	I	3.3V	
J1	68	SPI_A_MOSI	ECSPI1_MOSI	I	O	3.3V	
J1	70	SPI_A_SCLK	ECSPI1_SCLK	I	O	3.3V	
J1	56	SPI_B_SS0*1	ECSPI2_SS0	I	O	3.3V	
J1	58	SPI_B_MISO*1	ECSPI2_MISO	O	I	3.3V	
J1	60	SPI_B_MOSI*1	ECSPI2_MOSI	I	O	3.3V	
J1	62	SPI_B_SCLK*1	ECSPI2_SCLK	I	O	3.3V	

*1: Interface SPI_B is in parallel to the interface QSPI. QSPI is an assembly option. See chapter 4.5.
*2: SM: Slave Mode, MM: Master Mode

Table 6: SPI Interface

4.5 QSPI

The module can support optionally the QSPI interface. This feature comes in start with the HW Revision 1.30. On older versions of module there is no QSPI Interface support. The contacts for the QSPI interface are parallel to the contacts for SPI_B, so they cannot be used at the same time.

QSPI Interface can be available on modules with eMMC Flash. The NAND Flash versions do not have QSPI support.

For the QSPI assembly option please contact to our support team.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	52	QSPI_DATA0	NAND_DATA0	I/O	1.8V	
J1	54	QSPI_DATA1	NAND_DATA1	I/O	1.8V	
J1	56	QSPI_CS0	NAND_CE0_B	O	1.8V	
J1	58	QSPI_DATA2	NAND_DATA2	I/O	1.8V	
J1	60	QSPI_DATA3	NAND_DATA3	I/O	1.8V	
J1	62	QSPI_SCLK	NAND_ALE	O	1.8V	

Table 7: QSPI Interface

4.6 I2C

The module supports an I2C interface as I2C master. Devices on baseboard with other voltage need a level shifter. It's the preferred I2C for touch controller.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	4	I2C_A_SCL	I2C_1_SCL	O	3.3V	onboard pull-up 2.49k
J1	6	I2C_A_SDA	I2C_1_SDA	I/O	3.3V	onboard pull-up 2.49k
J1	3	I2C_B_SCL	I2C_2_SCL	O	3.3V	onboard pull-up 2.49k
J1	5	I2C_B_SDA	I2C_2_SDA	I/O	3.3V	onboard pull-up 2.49k
J1	1	I2C_B_IRQ	SAI3_TXFS	I	3.3V	
J1	40	I2C_C_SCL	I2C_3_SCL	O	3.3V	onboard pull-up 2.49k
J1	42	I2C_C_SDA	I2C_3_SDA	I/O	3.3V	onboard pull-up 2.49k
J1	48	I2C_D_SCL	I2C_4_SCL	O	3.3V	onboard pull-up 2.49k
J1	50	I2C_D_SDA	I2C_4_SDA	I/O	3.3V	onboard pull-up 2.49k

Table 8: I2C A/B/C/D Interface

Note: I2C_D is used on the module to control several devices (i.e. PMIC, RTC, Audio Codec, …). Therefore it's not possible to use this contacts as GPIO or any other function. For I2C_D, PicoCore is always the bus master. Please use I2C_A/B/C before using I2C_D.

4.7 Serial ports

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	14	UART_A_RTS	SAI2_TXFS	O	3.3V	Reserved for debug
J1	16	UART_A_CTS	SAI2_RXD0	I	3.3V	Reserved for debug
J1	18	UART_A_RXD	UART1_RXD	I	3.3V	Reserved for debug, onboard Pull-Up 100k
J1	20	UART_A_TXD	UART1_TXD	O	3.3V	Reserved for debug
J1	22	UART_B_RTS	SAI3_RXC	O	3.3V	
J1	24	UART_B_CTS	SAI3_RXD	I	3.3V	
J1	26	UART_B_RXD	UART2_RXD	I	3.3V	onboard Pull-Up 100k
J1	28	UART_B_TXD	UART2_TXD	O	3.3V	
J1	30	UART_C_RXD	UART3_RXD	I	3.3V	onboard Pull-Up 100k
J1	32	UART_C_TXD	UART3_TXD	O	3.3V	
J1	34	UART_D_RXD	UART4_RXD	I	3.3V	onboard Pull-Up 100k
J1	36	UART_D_TXD	UART4_TXD	O	3.3V	

Table 9: UART A/B/C/D Interface

We recommend to use UART_A for debugging and service only.

F&S standard software uses DCE mode for UART.

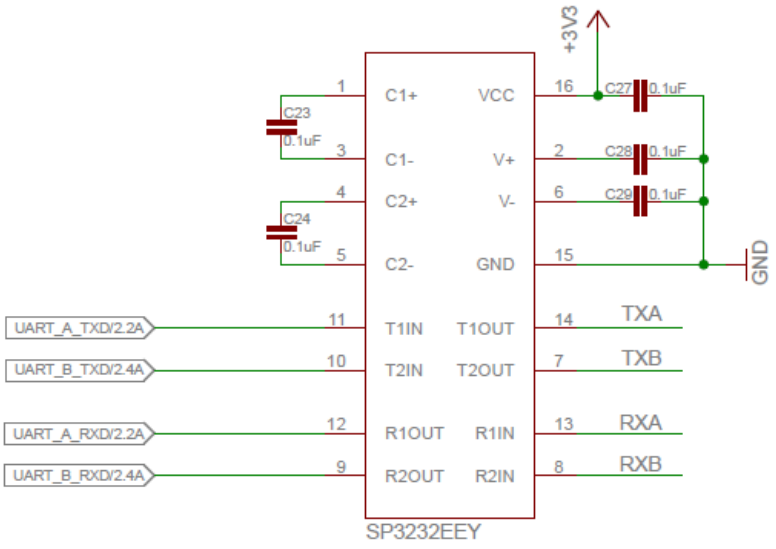

Figure 9: UART transceiver example

4.8 Ethernet

On the PicoCoreMX8MM module there are two options for the Ethernet interface. There is an assembly option to select between RGMII interface and 1x Gbit LAN.

The only difference between these two modules is their Gbit Ethernet PHY's.

PicoCore™MX8MM/MN → Qualcomm Atheros AR8035

PicoCore™MX8MMr2/MNr2 → Realtek RTL8211F/D

4.8.1 Ethernet RGMII Interface

Without Ethernet Switch: The module supports one 10/100/1000Mbit LAN interface via RGMII signals. The RGMII signals can be reached from the B2B Connector. An external Ethernet-Phy (i.e. AR8035) or an external Ethernet switch is required.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	1	ETH_A_D1_P	ENET_MDC	O	1.8V	
J2	3	ETH_A_D1_N	ENET_MDIO	I/O	1.8V	
J2	5	ETH_A_D2_P	RGMII_TX_CTL	O	1.8V	
J2	7	ETH_A_D2_N	RGMII_TXC	O	1.8V	
J2	9	ETH_A_D3_P	RGMII_TXD0	O	1.8V	
J2	11	ETH_A_D3_N	RGMII_TXD1	O	1.8V	
J2	13	ETH_A_D4_P	RGMII_TXD2	O	1.8V	
J2	15	ETH_A_D4_N	RGMII_TXD3	O	1.8V	
J2	23	ETH_B_D1_P	RGMII_RX_CTL	I	1.8V	
J2	25	ETH_B_D1_N	RGMII_RXC_R	I	1.8V	
J2	27	ETH_B_D2_P	RGMII_RXD0	I	1.8V	
J2	29	ETH_B_D2_N	RGMII_RXD1	I	1.8V	
J2	31	ETH_B_D3_P	RGMII_RXD2	I	1.8V	
J2	33	ETH_B_D3_N	RGMII_RXD3	I	1.8V	
J2	35	ETH_B_D4_P	ETH_SW_RST	O	3.3V	Eth Switch/PHY Reset
J2	37	ETH_B_D4_N	ETH_SW_INTn	I	3.3V	Eth Switch/PHY Interrupt, active low

Table 10: Ethernet Interface RGMII Signals (no Ethernet PHY)

4.8.2 Ethernet Interface 1x GBit LAN

With Ethernet PHY: The module can support one 10/100/1000Mbit LAN Interface. In this case the module comes with the Atheros AR8035 Ethernet PHY.

Ethernet data signals are connected as 100-Ohm differential pairs.

	Pin	Signal	AR8035 Pad	I/O	Voltage	Remarks
J2	1	ETH_A_D1_P	TXRXP_A	I/O	1.2V	Ethernet A Data 1+
J2	3	ETH_A_D1_N	TXRXM_A	I/O	1.2V	Ethernet A Data 1-
J2	5	ETH_A_D2_P	TXRXP_B	I/O	1.2V	Ethernet A Data 2+
J2	7	ETH_A_D2_N	TXRXM_B	I/O	1.2V	Ethernet A Data 2-
J2	9	ETH_A_D3_P	TXRXP_C	I/O	1.2V	Ethernet A Data 3+
J2	11	ETH_A_D3_N	TXRXM_C	I/O	1.2V	Ethernet A Data 3-
J2	13	ETH_A_D4_P	TXRXP_D	I/O	1.2V	Ethernet A Data 4+
J2	15	ETH_A_D4_N	TXRXM_D	I/O	1.2V	Ethernet A Data 4-
J2	17	ETH_A_LED	LED1_0	O	3.3V	Ethernet A LED indicator*[2]
J2	21	ETH_B_LED		O	3.3V	WLAN_LED*[1]
J2	23	ETH_B_D1_P	N.C.	X		Not connected can be left open
J2	25	ETH_B_D1_N	N.C.	X		
J2	27	ETH_B_D2_P	N.C.	X		
J2	29	ETH_B_D2_N	N.C.	X		
J2	31	ETH_B_D3_P	N.C.	X		
J2	33	ETH_B_D3_N	N.C.	X		
J2	35	ETH_B_D4_P	N.C.	X		
J2	37	ETH_B_D4_N	N.C.	X		

Table 11: 1x Gigabit Ethernet Interface with Ethernet Switch

*[1]: ETH_B_LED is used for WLAN Activity LED (if WLAN mounted, else N.C.)

*[2]: For PicoCore™MX8MMr2/MNr2 with Realtek RTL8211F/D the Signal “ETH_A_LED” is inverted.

This component is optional and not mounted in all configurations. Please contact sales to get more information.

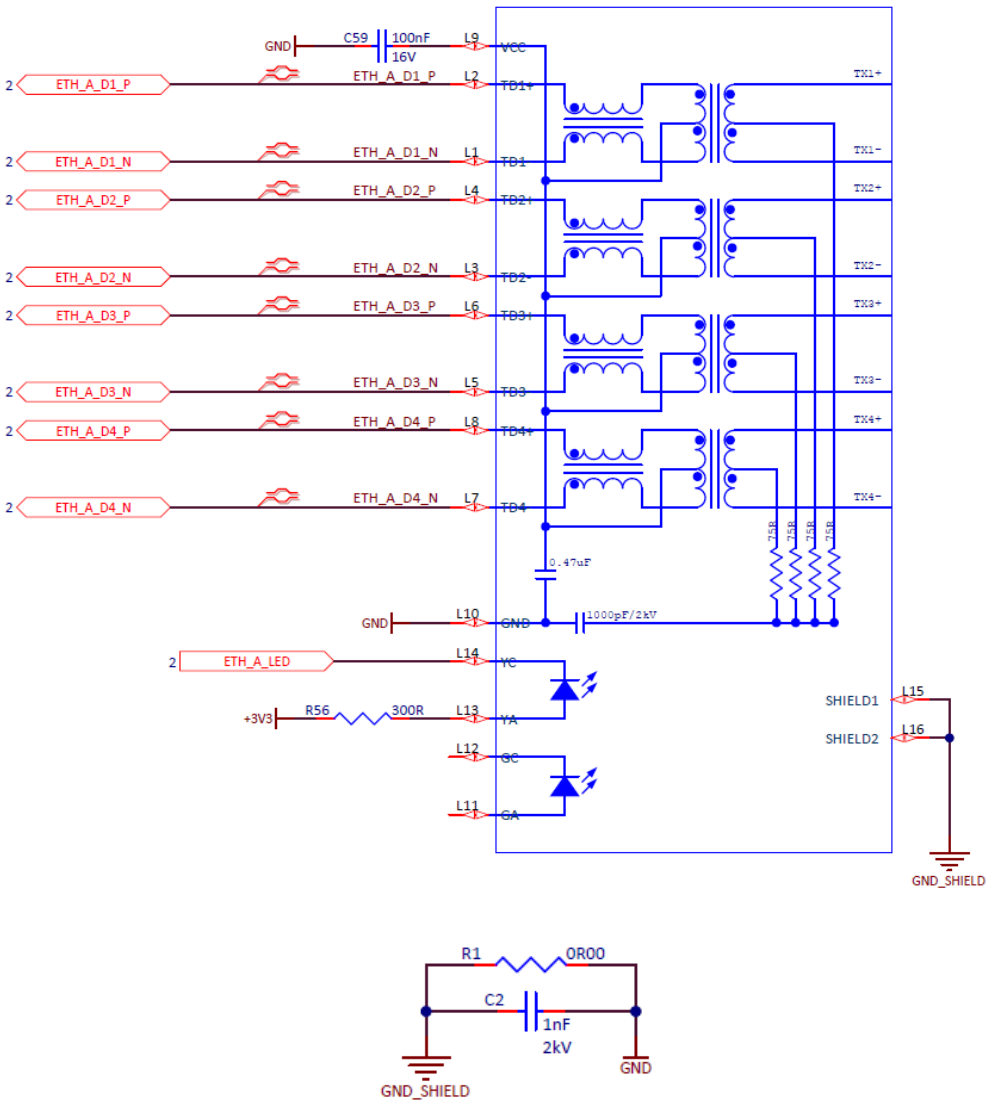

Figure 10: LAN output example

4.9 Audio

The PicoCoreMX8MM module can support audio interface either directly via I2S signals or with an external audio codec IC. The audio codec NXP SGTL5000 can be mounted on the module optionally. In this case the module can also support the MIC function.

AUDIO_A_VCC is supplied from the PMIC on PicoCore module as default. For a better and smoother audio quality, an external low-noise power supply (e.g. LDO) can be used. AUDIO_A_GND is connected to GND on PicoCore module as default. There is a mounting option to use external GND for the analogue part of the audio codec. Please contact us to have the right assembly option for AUDIO_A_VCC and/or AUDIO_A_GND.

	Pin	Signal	I/O	Voltage	Description
J2	2	AUDIO_A_VCC	I	3.3V/3V	Optional: Noise reduced external power supply for audio codec. Default: Onboard connection to 3.3V
J2	4	AUDIO_A_GND	I		Optional: Noise reduced external power supply for audio codec. Default: Onboard connection to GND
J2	6	AUDIO_A_LOUT_L	O	VCC_AUD	
J2	8	AUDIO_A_LOUT_R	O	VCC_AUD	
J2	10	AUDIO_A_MIC	I	VCC_AUD	
J2	12	AUDIO_A_LIN_L	I	VCC_AUD	
J2	14	AUDIO_A_LIN_R	I	VCC_AUD	
J2	18	AUDIO_A_HP_L	O	VCC_AUD	
J2	20	AUDIO_A_HP_R	O	VCC_AUD	
J2	22	AUDIO_A_HP_GND	O		Never connect to GND!

Table 12: Audio Interface (with Codec)

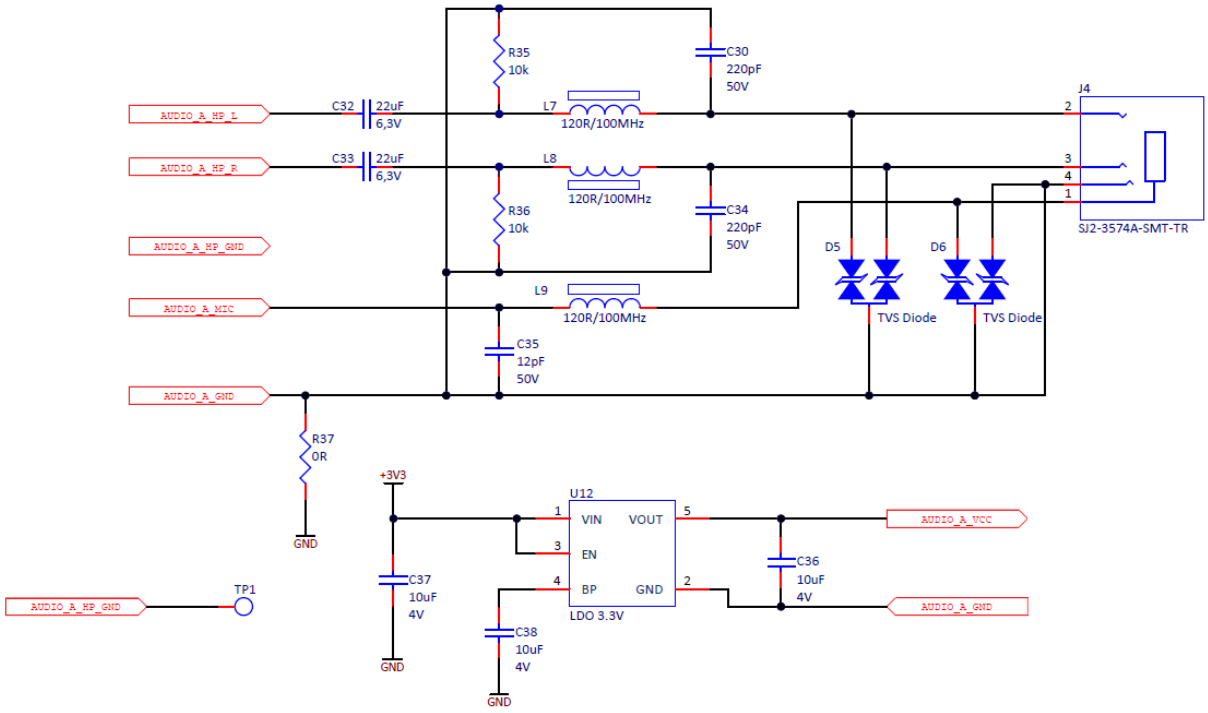

Figure 11: Headphone-Out Mic-In Example Circuit

	Pin	Signal	I/O	Voltage	Description
J2	2	N.C.	I		Do not connect
J2	4	N.C.	I		Do not connect
J2	6	I2S_SCLK	O	3.3V	
J2	8	I2S_LRCLK	O	3.3V	
J2	10	N.C.	X		Do not connect
J2	12	I2S_MCLK	O	3.3V	
J2	14	N.C.	X		Do not connect
J2	18	I2S_DOUT	O	3.3V	
J2	20	I2S_DIN	I	3.3V	
J2	22	N.C.	X		Do not connect

Table 13: Audio Interface (without Codec)

4.10 PCIE Interface

The PicoCoreMX8MM module supports single lane PCI Express Gen 2. The interface can work as root complex or endpoint (Dual mode operation).

mPCIe Interface is only supported with i.MX8M Mini Processor based modules.

Modules with i.MX8M Nano Processor do not have mPCIe option and the related pins on the connectors are N.C!

	Pin	Signal	I/O	Voltage	Description
J1	77	mPCIE_CTX_P	O		PCIe Transmit Data+
J1	79	mPCIE_CTX_N	O		PCIe Transmit Data-
J1	83	mPCIE_CRX_P	I		PCIe Receive Data+
J1	85	mPCIE_CRX_N	I		PCIe Receive Data-
J1	89	mPCIE_CLK_P	I/O		PCIe Clock+
J1	91	mPCIE_CLK_N	I/O		PCIe Clock-
J1	95	mPCIE_PERST	O		PCIe reset output
J1	97	mPCIE_WAKE	I		PCIe wakeup input

Table 14: PCIE Interface

4.11 MIPI DSI / LVDS Interface

The module supports one quad lane MIPI DSI interface up to 800 Mbps.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	17	DSI_A_CLK_P	MIPI_DSI_CLK_P	O	1.2V/200mV*[1]	
J1	19	DSI_A_CLK_N	MIPI_DSI_CLK_N	O	1.2V/200mV*[1]	
J1	23	DSI_A_DATA0_P	MIPI_DSI_D0_P	O	1.2V/200mV*[1]	
J1	25	DSI_A_DATA0_N	MIPI_DSI_D0_N	O	1.2V/200mV*[1]	
J1	29	DSI_A_DATA1_P	MIPI_DSI_D1_P	O	1.2V/200mV*[1]	
J1	31	DSI_A_DATA1_N	MIPI_DSI_D1_N	O	1.2V/200mV*[1]	
J1	35	DSI_A_DATA2_P	MIPI_DSI_D2_P	O	1.2V/200mV*[1]	
J1	37	DSI_A_DATA2_N	MIPI_DSI_D2_N	O	1.2V/200mV*[1]	
J1	41	DSI_A_DATA3_P	MIPI_DSI_D3_P	O	1.2V/200mV*[1]	
J1	43	DSI_A_DATA3_N	MIPI_DSI_D3_N	O	1.2V/200mV*[1]	
J1	47	DSI_B_CLK_P	N.C.	O		
J1	49	DSI_B_CLK_N	N.C.	O		
J1	53	DSI_B_DATA0_P	N.C.	O		
J1	55	DSI_B_DATA0_N	N.C.	O		
J1	59	DSI_B_DATA1_P	N.C.	O		
J1	61	DSI_B_DATA1_N	N.C.	O		
J1	65	DSI_B_DATA2_P	N.C.	O		
J1	67	DSI_B_DATA2_N	N.C.	O		
J1	71	DSI_B_DATA3_P	N.C.	O		
J1	73	DSI_B_DATA3_N	N.C.	O		

Table 15: MIPI-DSI Interface

*[1]: 1.2V in single-ended mode, approx. 200mV in differential mode

On the module there is a mounting option to get dual channel LVDS (up to 1920x1200 24-bit) instead of MIPI-DSI. In this case the module comes with Toshiba TC358775XBG MIPI-DSI to LVDS converter chip (Comes with HW Version 1.30).

Old HW Versions have just one channel LVDS. (Toshiba TC358775XBG)

	Pin	Signal	Function	I/O	Voltage	Remarks
J1	17	DSI_A_CLK_P	LVDS0_CLK_DP	O	1.2V/200mV*[1]	
J1	19	DSI_A_CLK_N	LVDS0_CLK_DN	O	1.2V/200mV*[1]	
J1	23	DSI_A_DATA0_P	LVDS0_TX0_DP	O	1.2V/200mV*[1]	
J1	25	DSI_A_DATA0_N	LVDS0_TX0_DN	O	1.2V/200mV*[1]	
J1	29	DSI_A_DATA1_P	LVDS0_TX1_DP	O	1.2V/200mV*[1]	
J1	31	DSI_A_DATA1_N	LVDS0_TX1_DN	O	1.2V/200mV*[1]	
J1	35	DSI_A_DATA2_P	LVDS0_TX2_DP	O	1.2V/200mV*[1]	
J1	37	DSI_A_DATA2_N	LVDS0_TX2_DN	O	1.2V/200mV*[1]	
J1	41	DSI_A_DATA3_P	LVDS0_TX3_DP	O	1.2V/200mV*[1]	
J1	43	DSI_A_DATA3_N	LVDS0_TX3_DN	O	1.2V/200mV*[1]	
J1	47	DSI_B_CLK_P	LVDS1_CLK_DP	O	1.2V/200mV*[1]	
J1	49	DSI_B_CLK_N	LVDS1_CLK_DN	O	1.2V/200mV*[1]	
J1	53	DSI_B_DATA0_P	LVDS1_TX0_DP	O	1.2V/200mV*[1]	
J1	55	DSI_B_DATA0_N	LVDS1_TX0_DN	O	1.2V/200mV*[1]	
J1	59	DSI_B_DATA1_P	LVDS1_TX1_DP	O	1.2V/200mV*[1]	
J1	61	DSI_B_DATA1_N	LVDS1_TX1_DN	O	1.2V/200mV*[1]	
J1	65	DSI_B_DATA2_P	LVDS1_TX2_DP	O	1.2V/200mV*[1]	
J1	67	DSI_B_DATA2_N	LVDS1_TX2_DN	O	1.2V/200mV*[1]	
J1	71	DSI_B_DATA3_P	LVDS1_TX3_DP	O	1.2V/200mV*[1]	
J1	73	DSI_B_DATA3_N	LVDS1_TX3_DN	O	1.2V/200mV*[1]	

Table 16: 2 Channel LVDS Interface

*[1] 1.2V in single-ended mode, approx. 200mV in differential mode

4.12 MIPI CSI Interface

The module supports quad lane MIPI CSI interface.

	Pin	Signal	I/O	Voltage	Description
J1	80	CSI_DATA0_P	I		CSI Input Data0+
J1	82	CSI_DATA0_N	I		CSI Input Data0-
J1	86	CSI_DATA1_P	I		CSI Input Data1+
J1	88	CSI_DATA1_N	I		CSI Input Data1-
J1	92	CSI_DATA2_P	I		CSI Input Data2+
J1	94	CSI_DATA2_N	I		CSI Input Data2-
J1	98	CSI_DATA3_P	I		CSI Input Data3+
J1	100	CSI_DATA3_N	I		CSI Input Data3-
J1	74	CSI_CLK_P	I		CSI Input Clock+
J1	76	CSI_CLK_N	I		CSI Input Clock-

Table 17: MIPI CSI Interface

4.13 WLAN and Bluetooth Interface

The PicoCore™MX8MM/MN modules contain a certified high performance WLAN and Bluetooth module.

The WLAN/BT module is an assembly option.

The module is based on NXP W8997 chip, having CE, FCC, IC, NCC, AU/NZ, India, Japan (pre) certificates. Please contact support@fs-net.de for additional information about process of certification.

The module offers:

- IEEE802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, Bluetooth 3.0 and Bluetooth 5.0 (supports low Energy)

Information about Bluetooth (QDID):

Please refer to the following BT QDID info for 88W8997 (AW-CM276NF).

QDID : D046929

https://launchstudio.bluetooth.com/ListingDetails/91724

If Bluez-5.37 will be used, the QDID from NXP can be used

https://launchstudio.bluetooth.com/ListingDetails/92249

Customer can use this QDIDs to create their device QDID.

Note: In case WLAN/BT module is mounted only one external SD card interface (SD_A) is available.

This component is optional and not mounted in all configurations. Please contact sales to get more information.

4.14 CAN FD Interface

The module can also support the CAN FD Interface with an optional external controller.

If this option is selected, the module comes with MCP2518FD CAN controller IC which uses one of SPI channel (SPI_A). Then just one SPI channel (SPI_B) is available instead of two.

	Pin	Signal	Function	I/O	Voltage	Remarks
J1	10	CAN_RX	RXCAN	I	3.3V	CAN Receive Data
J1	12	CAN_TX	TXCAN	O	3.3V	CAN Transmit Data

Table 18: CAN FD Pin Layout

This component is optional and not mounted in all configurations. Please contact sales to get more information.

4.15 GPIOs

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pull-ups or pull-downs are configurable by software, but they are not available at board start-up. On a non-powered board it's not allowed to have a voltage on one of the GPIO contacts. Also a higher voltage as the announced IO power is not allowed.

Some of the GPIOs are feature optional. The usage and the availability can be changed with the assembly options. Please contact us to have the right assembly option.

On the **PicoCoreMX8MN** Module, GPIO_J2_69, GPIO_J2_73, GPIO_J2_77, GPIO_J2_79 are shared with CAN-FD Transceiver. These GPIOs are free only if the CAN-FD transceiver is not mounted on module.

On the **PicoCoreMX8MN** Module, GPIO_J2_83, GPIO_J2_85 are shared with the LVDS Bridge. These GPIOs are free only if the LVDS Bridge is not mounted on module.

On the **PicoCoreMX8MN** Module, GPIO_J2_87 is shared with the WLAN module. This GPIO is free only if the WLAN chip is not mounted on module.

On the **PicoCoreMX8MN** Module, GPIO_J2_89 is shared with the SE050 security chip. This GPIO is free only if the security chip is not mounted on module.

	Pin	Standard	CPU Pad PicoCoreMX8MM	CPU Pad PicoCoreMX8MN	Voltage	Remarks
J1	2	GPIO_J1_2	GPIO1_IO13	GPIO1_IO13	3.3V	
J1	7	GPIO_J1_7	GPIO1_IO01	GPIO1_IO01	3.3V	Optional PWM (PWM1)
J1	44	GPIO_J1_44	GPIO1_IO08	GPIO1_IO08	3.3V	
J1	46	GPIO_J1_46	GPIO1_IO09	GPIO1_IO09	3.3V	
J1	52	GPIO_J1_52	GPIO1_IO10	GPIO1_IO10	3.3V	
J1	54	GPIO_J1_54	GPIO1_IO11	GPIO1_IO11	3.3V	Only Nano CPU: Optional PWM (PWM2)
J2	63	PWM	SPDIF_EXT_CLK	SPDIF_EXT_CLK	3.3V	PWM Output (PWM1)
J2	65	GPIO_J2_65	SAI1_TXD7	SAI2_MCLK	3.3V	
J2	67	GPIO_J2_67	SAI1_TXD6	N.C.	3.3V	
J2	69	GPIO_J2_69	SAI1_TXD4	SAI2_TXC*	3.3V	*shared with CAN-FD
J2	73	GPIO_J2_73	SAI1_TXD5	SAI2_TXD0*	3.3V	*shared with CAN-FD
J2	75	GPIO_J2_75	SAI1_RXD5	N.C.	3.3V	
J2	77	GPIO_J2_77	SAI1_RXD6	SAI2_RXFS*	3.3V	*shared with CAN-FD
J2	79	GPIO_J2_79	SAI1_RXD4	SAI2_RXC*	3.3V	*shared with CAN-FD
J2	83	GPIO_J2_83	SAI1_MCLK	GPIO_IO15*	3.3V	*shared with LVDS
J2	85	GPIO_J2_85	SAI1_RXD7	SAI3_TXFS*	3.3V	*shared with LVDS
J2	87	GPIO_J2_87	SAI1_TXC	SAI3_TXC*	3.3V	*shared with WLAN
J2	89	GPIO_J2_89	SAI1_RXD0	SAI3_TXD*	3.3V	*shared with SE050

Table 19: GPIO Table

4.16 JTAG

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	93	JTAG_TCK	JTAG_TCK[*1]	I	1.8V	JTAG_TCK
J2	95	JTAG_TMS	JTAG_TMS[*1]	I	1.8V	JTAG_TMS
J2	97	JTAG_TDI	JTAG_TDI[*1]	I	1.8V	JTAG_TDI
J2	99	JTAG_TDO	JTAG_TDO[*1]	O	1.8V	JTAG_TDO

Table 20: JTAG Interface

- For debug only
- Leave unconnected, if you don't use JTAG
- Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU

5 Power and Power Control Pins

	Pin	Signal	I/O	Description
J2	24 26 28	VDD_VIN	I	Main Power supply input please refer chapter 10 Electrical characteristic
J2	30 32 34	GND	I	Main Power supply Ground input
J2	36	VDD_VBAT	I	RTC battery input; tie to 3.0V please refer chapter 10 Electrical characteristic
J2	38	RESERVED	X	(formerly VDD_SNVS) Please leave this pin floating (N.C.)
J2	40	VDD_3V3	O	20mA output from on module DCDC powered from VIN Please do not use for power supply of carrier board!
J2	52	SD_A_VCC	I	SDHC power output; 3.3V/ 1.8V
J2	51	USB_OTG_VBUS	I	USB Phy voltage input; 5V
J2	41	USB_H_VBUS	I	USB Phy voltage input; 5V
J2	42	RESETIN	I	Power on reset input; 10k PU; 1.8V* (3.3V on Rev. 1.00)
J2	44	PMIC_STBY	O	Active high for going to SUSPEND state
J2	46	PMIC_ON_REQ	O	Active high for going to RUN state
J2	48	ON_OFF	I	CPU On/Off control pin, can be used with an external button

Table 21: Power and Power Control

By using a battery for VBAT you have to follow regulation rules. Please check with your test laboratory. It's possible to use a supercap instead.

VDD_3V3 is a 3.3V @20mA output. It's generated from the internal PMIC and powered from VIN. Can be used as "Enable Signal" for the power regulators on baseboard. Please do not use VDD_3V3 as power supply for carrier board.

RESETIN is the reset input for the module. RESETIN only resets the CPU. In the event of a power failure, VDD_VIN must be switched off and on to avoid latch-up effects.

PMIC_STBY_REQ is set HIGH when the CPU is in standby mode. This allows to switch off peripheral functions and save more power. Wakeup from standby mode needs support by the driver, you have to check.

The GND contacts which are given in the table above are the power ground contacts for VDD_VIN. For a better EMC performance it is highly recommended to connect all GND contacts to GND on the carrier board (not just the power ground contacts).

6 Boot Mode

The CPU of PicoCore has fuses to configure the default boot device. By default it is eMMC or NAND, depending from the soldered mass storage flash memory.

With pin 50 of J2 “BOOTSEL” it is possible to switch between “boot from internal fuses” and “boot from USB serial download”.

So you have the following two boot options:

Boot Device Select	BOOTSEL pin of PicoCore
Boot from internal fuses	Leave open
USB Serial Download	Connect to GND

Table 22: Boot Modes of PicoCore

7 Flash

PicoCoreMX8MM/MN modules can be shipped with SLC NAND Flash or MLC eMMC. By default fuses of i.MX8M Mini are configured so that PicoCoeMX8MM boots from the assembled flash memory.

Please contact support for other boot options.

7.1 NAND Flash

The board implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored two times in flash memory
- Flash data protected by 32 bit ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system

7.2 eMMC

If mounted instead NAND an eMMC v4.41 or higher with 4GB or more is mounted from several manufacturer.

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

8 RTC

There is a NXP PCF85263ATL or compatible implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

9 Secure Authenticator IC

The secure tamper-resistant authentication IC NXP SE050 offers a strong cryptographic solution intended to be used by device manufacturers to prove the authenticity of their genuine products. It can be used for brand protection, revenue protection, and or customer safety.

For more information visit NXPs web side.

SE050 Quick start guide: https://www.nxp.com/docs/en/application-note/AN13027.pdf

This component is optional and not mounted in all configurations. Please contact sales to get more information.

10 Electrical characteristic

10.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IOs	-0.3	OVDD*+0.3	V
Voltage on any IO with VDD_VIN off		0.3	V
USB VBUS	-0.3	5.6	V
Maximum power consumption VDD_VBAT at 85°C		0.6	µA
Maximum output current 3.3V		20	mA

Table 23: Absolute Maximum Ratings

10.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Max	Unit
VDD_VIN	Module main power		4.5	5.5	V
VDD_VBAT	RTC power		0.9	5.5	V
VDD_SNVS	SNVS voltage in		4.5	5.5	V
USB_OTG*_VBUS	USB supply voltage		4.4	5.5	V
OVDD	On module 3.3V from on module PMIC, delayed after VDD_SNVS		3.15	3.45	V
VDD_3V3	3.3V output for power enable on carrier board		OVDD	OVDD	V
V_{ih}	High Level Input Voltage		0.7*OVDD	OVDD	V
V_{il}	Low Level Input Voltage		0	0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15		V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA		0.15	V
I_o	Output current IOs	3.3V		5	mA
I_{VBAT}	Current consumption VBAT			0.22[*1]	µA

Table 24: DC Electrical Characteristics

[*1] Low current: typical 0.22 µA at VDD = 3.3 V and Tamb = 25 °C

11 Thermal Specification

This Embedded Module is a high-performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors (housing, power consumption, heat spreader, airflow and many others).

In order to keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
- For reducing the heat dissipation, CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS) as well as “Thermal throttling”, by an integrated temperature sensor.
    - The integrated sensor measures the die-temperature and lowers CPU clock or shut down CPU if needed.
    - DVFS lowers CPU clock and core voltage in accordance with the performance needed from the application.

For optimal use of DVFS, modify your software to only use peak performance only for short times.

The housing has big influence on the heat dissipation. There are many points to analyze:

- Is there the option of dissipating heat to the housing?
- Is there a possibility that the air can circulate in the housing?
- Is an active cooling possible?

The surrounding heat has a big effect to the temperature of the system.

Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction!

The following table shows nominal thermal specification of the module:

Operating Ranges	Min	Typ.	Max	Unit
Consumer Range Environmental Temperature	0		+70	°C
Consumer Range CPU Junction Temperature	0		+95	°C
Industrial Range Environmental Temperature (I)	-20		+85	°C
Industrial Range CPU Junction Temperature (I)	-40*2		+105	°C
Extended Industrial Range Environmental Temperature (XI)	-40*2		+85	°C
Extended Industrial Range CPU Junction Temperature (XI)	-40*2		+105	°C
Junction to Package Top (Ψ_{JT}) - **i.MX8M Mini & Nano**		0.2		°C /W

Note 1: Maximum junction temperature of the CPU is 95°C /105°C. In this case cooling is necessary and highly recommended for operations near the limits. See also: Power Consumption and Cooling

Please get in contact with F&S for recommended cooling solutions.

Note 2: MIPI to LVDS Bridge and WLAN/BT is -30°C to +85°C only. These components are not critical for the booting operation.

Note 3: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN12468 (https://www.nxp.com/docs/en/application-note/AN12468.pdf)

12 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

13 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

14 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

15 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **10 Watt**. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **3Watt** to **8Watt**. Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

For the optimal cooling performance we recommend to use F&S heat spreader set MHS.PC100.1. For more information please contact with us.

15.1 Power Consumption in Suspend to RAM

PicoCoreMX8MM-V3:
i.MX8M Mini@1.8GHz, 512MB SLC NAND, 1GB LPDDR4, 1x GBit LAN, WLAN/BT, MIPI2LVDS Bridge

Power consumption: 125mW for the full board.

The purpose of the above value is only to give you an idea about the power consumption in "suspend to ram" mode. The value is for the whole board.

16 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage we recommend vacuum dry packs.

17 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

18 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

19 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 12: Matrix Code Sticker

20 Appendix

Important Notice

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