Hardware Documentation

*PicoCore™MX8Mx**
for HW Revision 1.20

**DDR3L Version of PicoCore™MX8MM / MX8MN*

Preliminary

Version 008
(2021-02-26)

Elektronik Systeme

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About This Document

This document describes how to use the PicoCore™MX8Mx board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

This document is written for the PicoCoreMX8MM and PicoCoreMX8MN modules, which have DDR3L DRAM and do not have a WLAN/BT connectivity. The related boards are given below in the table.

Related Modules
PicoCore™MX8MM-V5-LIN
PicoCore™MX8MM-V6-LIN
PicoCore™MX8MN-V1-LIN
PicoCore™MX8MN-V5-LIN

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
14.02.2020	001	All		-	Initial Version	MD
27.05.2020	002	All	A	2	Addition of new PCB variants and pin1 marker for the J1 and J2 connectors	MD
26.06.2020	003	All	M	3.1	Correction of SD_A_RST and SD_B_RST Pin function	MD
21.07.2020	004	All	M	4.4	Change of Ethernet switch	MD
21.07.2020	004	All	M	4.10	Correction of the mPCIe table	MD
21.07.2020	004	All	M	3.1, 4.7	correction of UART_A_RTS/UART_A_CTS&UART_B_RTS/UART_B_CTS pins on connector J1	MD
16.09.2020	005	All	M	4.1, 4.2, 4.3, 4.4, 14	Updated figures (schematic examples), Added Information for the Audio Supply Voltage (AUDIO_A_VCC) Updated power consumptions	MD
13.10.2020	006	All	M	All	Major corrections and additional informations	MD
28.10.2020	007	All	M	4, 8	Important information for Pin J2_38 (former VDD_SNVS)	MD
26.02.2021	008	All	A,M M M	4.5, 7 4.14 3.1	New HW Version, support for QSPI, new security chip SE050 Changes on GPIO table Corrections on the B2B connector (CPU Pads)	MD

V	Version
A,M,R	Added, Modified, Removed
Au	Author

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1 Block diagram

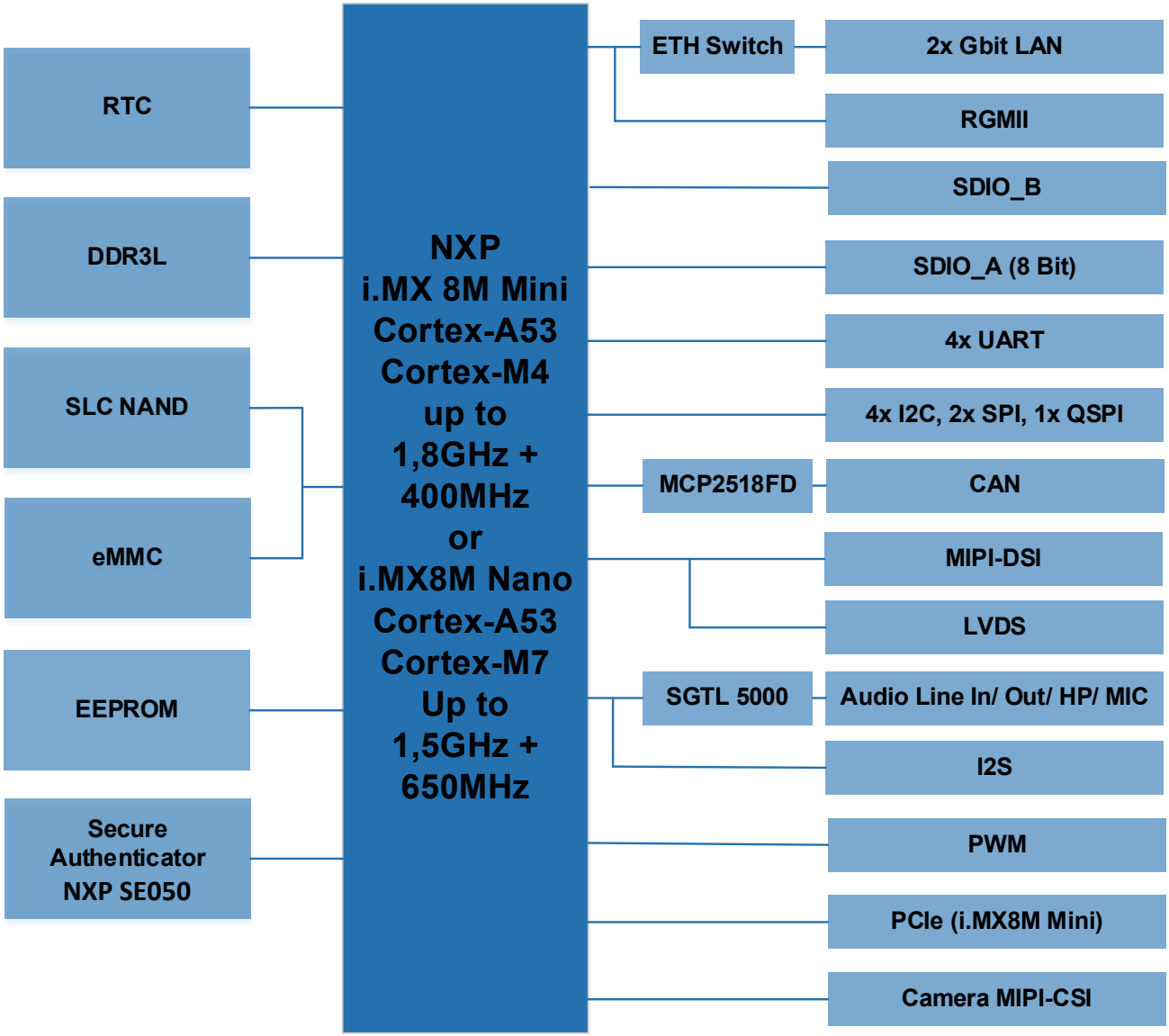

Figure 1: Block Diagram

2 Mechanical Dimension

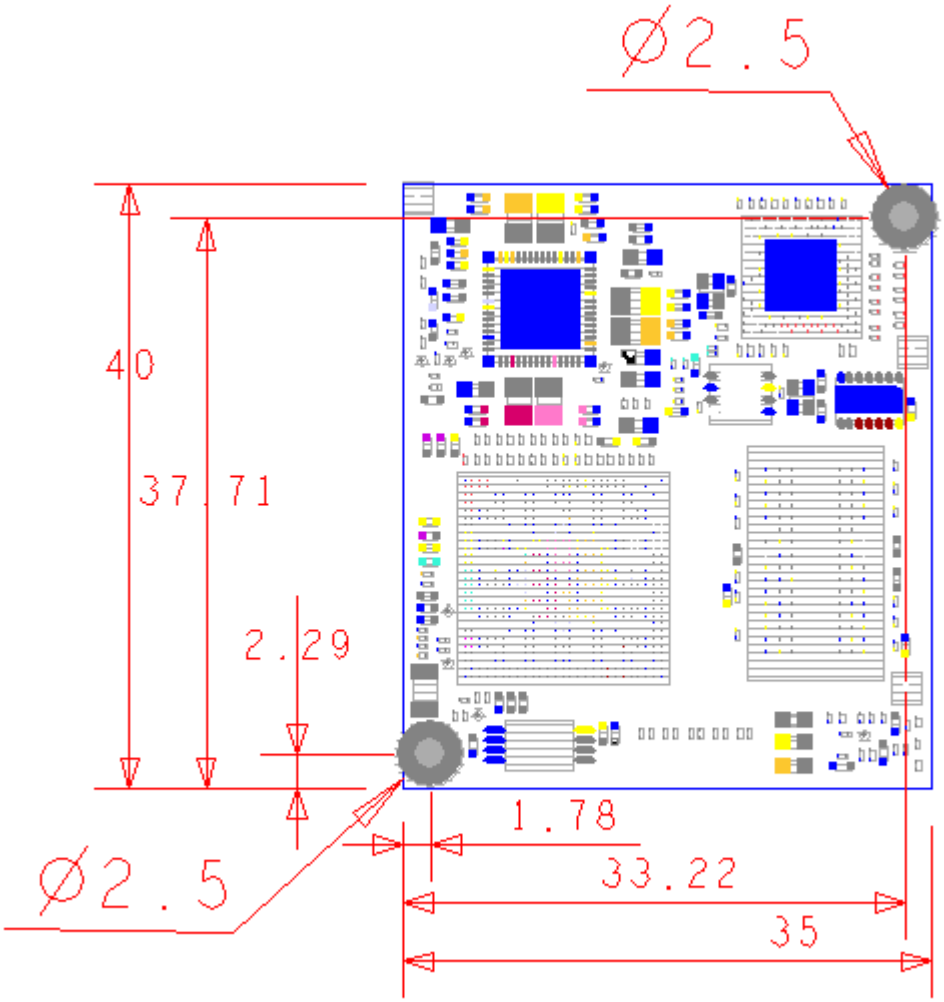

Figure 2: Mechanical Dimension Top

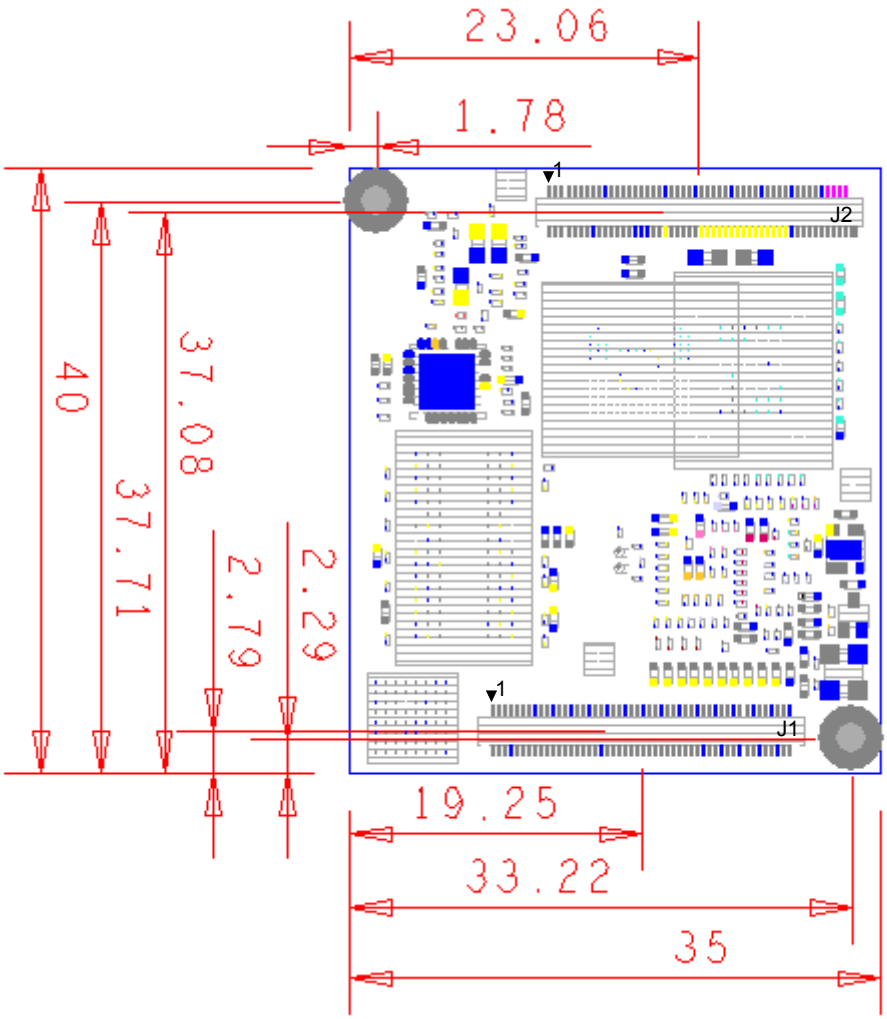

Figure 3: Mechanical Dimension Bottom

Dimensions	Description
Size	40mm x 35mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	Max. 5mm
Height of the parts on the bottom side	Max. 1.4mm
Weight	14gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

2.1 SMT Steel Spacer

For mounting we recommend SMT Steel Spacer from supplier “Würth Elektronik” order number “9774015243R”.

This part is in F&S stock and can be ordered via web shop.

Data sheet and 3D model (STP) is available on our website.

If you use different stacking high, you have to change the Spacer.

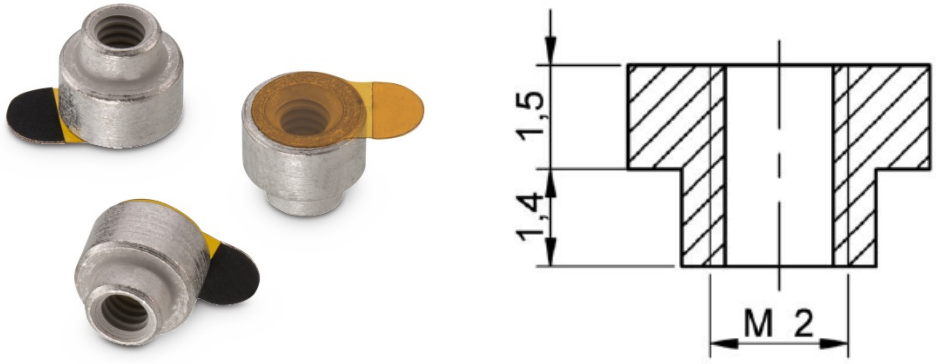

Figure 4: WE SMT Steel Spacer

3 Interface and signal description

3.1 B2B connectors

PicoCoreMX8Mx is using two 100 pin connectors from manufacturer Hirose.

Part number: DF40C-100DP-0.4V

Part number counterpart: DF40C-100DS-0.4V

With this combination you get minimal stacking height of 1,5mm. Another possible stacking height by using different counterpart connector is: 3mm. The connector with 1,5mm stacking height is available at F&S and can be ordered in web shop.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	1	I2C_B_IRQ	SAI3_MCLK	I	3.3V	
J1	2	GPIO_J1_2	GPIO1_IO13	I/O	3.3V	Standard GPIO
J1	3	I2C_B_SCL	I2C2_SCL	O	3.3V	
J1	4	I2C_A_SCL	I2C4_SCL	O	3.3V	
J1	5	I2C_B_SDA	I2C2_SDA	I/O	3.3V	
J1	6	I2C_A_SDA	I2C4_SDA	I/O	3.3V	
J1	7	GPIO_J1_7	GPIO1_IO01	I/O	3.3V	Standard GPIO
J1	8	GND		PWR	GND	
J1	9	BL_ON	SPDIF_TX	O	3.3V	
J1	10	CAN_RX		I	3.3V	*1
J1	11	BL_PWM	SPDIF_RX	O	3.3V	
J1	12	CAN_TX		O	3.3V	*1
J1	13	VLCD_ON	SAI3_TXD	O	3.3V	*2 MIPI-DSI/LVDS1
J1	14	UART_A_RTS	SAI2_TXFS	O	3.3V	
J1	15	GND		PWR	GND	
J1	16	UART_A_CTS	SAI2_RXD0	I	3.3V	
J1	17	DSI_A_CLK_P	MIPI_DSI_CLK_P	O	1.2V/200mV	*2 MIPI-DSI/LVDS1
J1	18	UART_A_RXD	SAI2_RXC	I	3.3V	
J1	19	DSI_A_CLK_N	MIPI_DSI_CLK_N	O	1.2V/200mV	*2 MIPI-DSI/LVDS1
J1	20	UART_A_TXD	SAI2_RXFS	O	3.3V	
J1	21	GND		PWR	GND	
J1	22	UART_B_RTS	SAI3_RXC	O	3.3V	
J1	23	DSI_A_DATA0_P	MIPI_DSI_D0_P	O	1.2V/200mV	*2 MIPI-DSI/LVDS1
J1	24	UART_B_CTS	SAI3_RXD	I	3.3V	
J1	25	DSI_A_DATA0_N	MIPI_DSI_D0_N	O	1.2V/200mV	*2 MIPI-DSI/LVDS1
J1	26	UART_B_RXD	SAI3_TXFS	I	3.3V	

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	27	GND		PWR	GND	
J1	28	UART_B_TXD	SAI3_TXC	O	3.3V	
J1	29	DSI_A_DATA1_P	MIPI_DSI_D1_P	O	1.2V/200mV	*2 MIPI-DSI/LVDS1
J1	30	UART_C_RXD	UART4_RXD	I	3.3V	
J1	31	DSI_A_DATA1_N	MIPI_DSI_D1_N	O	1.2V/200mV	*2 MIPI-DSI/LVDS1
J1	32	UART_C_TXD	UART4_TXD	O	3.3V	
J1	33	GND		PWR	GND	
J1	34	UART_D_RXD	UART3_RXD	I	3.3V	
J1	35	DSI_A_DATA2_P	MIPI_DSI_D2_P	O	1.2V/200mV	*2 MIPI-DSI/LVDS1
J1	36	UART_D_TXD	UART3_TXD	O	3.3V	
J1	37	DSI_A_DATA2_N	MIPI_DSI_D2_N	O	1.2V/200mV	*2 MIPI-DSI/LVDS1
J1	38	GND		PWR	GND	
J1	39	GND		PWR	GND	
J1	40	I2C_C_SCL	I2C3_SCL	O	3.3V	
J1	41	DSI_A_DATA3_P	MIPI_DSI_D3_P	O	1.2V/200mV	*2 MIPI-DSI/LVDS1
J1	42	I2C_C_SDA	I2C3_SDA	I/O	3.3V	
J1	43	DSI_A_DATA3_N	MIPI_DSI_D3_N	O	1.2V/200mV	*2 MIPI-DSI/LVDS1
J1	44	GPIO_J1_44	GPIO1_IO00	I/O	3.3V	*7
J1	45	GND		PWR	GND	
J1	46	GPIO_J1_46	GPIO1_IO04	I/O	3.3V	*7
J1	47	DSI_B_CLK_P		O	1.2V/200mV	*2 LVDS2
J1	48	I2C_D_SCL	I2C1_SCL	O	3.3V	Shared I2C
J1	49	DSI_B_CLK_N		O	1.2V/200mV	*2 LVDS2
J1	50	I2C_D_SDA	I2C1_SDA	I/O	3.3V	Shared I2C
J1	51	GND		PWR	GND	
J1	52	GPIO_J1_52	GPIO1_IO08	I/O	3.3V	*7
J1	53	DSI_B_DATA0_P		O	1.2V/200mV	*2 LVDS2
J1	54	GPIO_J1_54	GPIO1_IO15	I/O	3.3V	*7
J1	55	DSI_B_DATA0_N		O	1.2V/200mV	*2 LVDS2
J1	56	SPI_B_SS0	UART2_TXD	I/O	3.3V	
J1	57	GND		PWR	GND	
J1	58	SPI_B_MISO	UART2_RXD	I/O	3.3V	
J1	59	DSI_B_DATA1_P		O	1.2V/200mV	*2 LVDS2
J1	60	SPI_B_MOSI	UART1_TXD	I/O	3.3V	
J1	61	DSI_B_DATA1_N		O	1.2V/200mV	*2 LVDS2
J1	62	SPI_B_SCLK	UART1_RXD	I/O	3.3V	
J1	63	GND		PWR	GND	
J1	64	SPI_A_SS0	ECSPI1_SS0	I/O	3.3V	

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	65	DSI_B_DATA2_P		O	1.2V/200mV	*2 LVDS2
J1	66	SPI_A_MISO	ECSPI1_MISO	I/O	3.3V	
J1	67	DSI_B_DATA2_N		O	1.2V/200mV	*2 LVDS2
J1	68	SPI_A_MOSI	ECSPI1_MOSI	I/O	3.3V	
J1	69	GND		PWR		GND
J1	70	SPI_A_SCLK	ECSPI1_SCLK	I/O	3.3V	
J1	71	DSI_B_DATA3_P		O	1.2V/200mV	*2 LVDS2
J1	72	GND		PWR		GND
J1	73	DSI_B_DATA3_N		O	1.2V/200mV	*2 LVDS2
J1	74	CSI_CLK_P	MIPI_CSI_CLK_P	I	1.8V	
J1	75	GND		PWR		GND
J1	76	CSI_CLK_N	MIPI_CSI_CLK_N	I	1.8V	
J1	77	MPCIE_CTX_P	PCIE_TXN_P	O		*3
J1	78	GND		PWR		GND
J1	79	MPCIE_CTX_N	PCIE_TXN_N	O		*3
J1	80	CSI_DATA0_P	MIPI_CSI_D0_P	I	1.8V	
J1	81	GND		PWR		GND
J1	82	CSI_DATA0_N	MIPI_CSI_D0_N	O	1.8V	
J1	83	MPCIE_CRX_P	PCIE_RXN_P	I		*3
J1	84	GND		PWR		GND
J1	85	MPCIE_CRX_N	PCIE_RXN_N	I		*3
J1	86	CSI_DATA1_P	MIPI_CSI_D1_P	I	1.8V	
J1	87	GND		PWR		GND
J1	88	CSI_DATA1_N	MIPI_CSI_D1_N	I	1.8V	
J1	89	MPCIE_CLK_P	PCIE_CLK_P	O		*3
J1	90	GND		PWR		GND
J1	91	MPCIE_CLK_N	PCIE_CLK_N	O		*3
J1	92	CSI_DATA2_P	MIPI_CSI_D2_P	I	1.8V	
J1	93	GND		PWR		GND
J1	94	CSI_DATA2_N	MIPI_CSI_D2_N	I	1.8V	
J1	95	MPCIE_PERST	SAI5_RXFS	O	3.3V	*3
J1	96	GND		PWR		GND
J1	97	MPCIE_WAKE	SAI5_RXC	I	3.3V	*3
J1	98	CSI_DATA3_P	MIPI_CSI_D3_P	I	1.8V	
J1	99	GND		PWR		GND
J1	100	CSI_DATA3_N	MIPI_CSI_D3_N	I	1.8V	

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	1	ETH_A_D1P		I/O		*4
J2	2	AUDIO_A_VCC		PWR	3V	*5 Optional
J2	3	ETH_A_D1N		I/O		*4
J2	4	AUDIO_A_GND		PWR	GND	*5 Optional
J2	5	ETH_A_D2P		I/O		*4
J2	6	AUDIO_A_LOUT_L		O		*5 Line-Out left
J2	7	ETH_A_D2N		I/O		*4
J2	8	AUDIO_A_LOUT_R		O		*5 Line-Out right
J2	9	ETH_A_D3P		I/O		*4
J2	10	AUDIO_A_MIC		I		*5 Microphone-In
J2	11	ETH_A_D3N		I/O		*4
J2	12	AUDIO_A_LIN_L		I		*5 Line-In left
J2	13	ETH_A_D4P		I/O		*4
J2	14	AUDIO_A_LIN_R		I		*5 Line-In right
J2	15	ETH_A_D4N		I/O		*4
J2	16	GND		PWR	GND	
J2	17	ETH_A_LED		O	3.3V	*4
J2	18	AUDIO_A_HP_L		O		*5 Headphone left
J2	19	GND		PWR	GND	
J2	20	AUDIO_A_HP_R		O		*5 Headphone right
J2	21	ETH_B_LED		O	3.3V	*4
J2	22	AUDIO_A_HP_GND		O		*5 Never connect to GND!
J2	23	ETH_B_D1P		I/O		*4
J2	24	VDD_VIN		PWR	5.0V	Supply Voltage Input
J2	25	ETH_B_D1N		I/O		*4
J2	26	VDD_VIN		PWR	5.0V	Supply Voltage Input
J2	27	ETH_B_D2P		I/O		*4
J2	28	VDD_VIN		PWR	5.0V	Supply Voltage Input
J2	29	ETH_B_D2N		I/O		*4
J2	30	GND		PWR	GND	
J2	31	ETH_B_D3P		I/O		*4
J2	32	GND		PWR	GND	
J2	33	ETH_B_D3N		I/O		*4
J2	34	GND		PWR	GND	
J2	35	ETH_B_D4P		I/O		*4
J2	36	VDD_VBAT		PWR	0.9V-5.5V	RTC battery Input
J2	37	ETH_B_D4N		I/O		*4
J2	38	RESERVED	X		X	Please leave N.C.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	39	GND		PWR	GND	
J2	40	VDD_3V3		O	3.3V	20mA output from on module DCDC powered from VIN
J2	41	USB_HOST_VBUS	USB2_VBUS	I	5.0V	*6
J2	42	RESETINN	P\W\R\O\N\	I	1.8V	Power on reset Input; onboard Pull-up 100k
J2	43	USB_HOST_DP	USB2_DP	I/O		*6
J2	44	PMIC_STBY	PMIC_STBY_REQ	O	1.8V	
J2	45	USB_HOST_DN	USB2_DN	I/O		*6
J2	46	PMIC_ON_REQ	PMIC_ON_REQ	O	1.8V	
J2	47	USB_HOST_PWRN	GPIO1_IO14	O	3.3V	*6
J2	48	ON_OFF	ONOFF	I	1.8V	On/Off Input for CPU
J2	49	GND		PWR	GND	
J2	50	BOOTSEL		I	1.8V	Service jumper; normally left open
J2	51	USB_OTG_VBUS	USB1_VBUS	I	5.0V	USB Phy voltage supply
J2	52	SD_A_VCC		O	1.8V / 3.3V	Selectable
J2	53	USB_OTG_PWRN	GPIO1_IO12	O	3.3V	
J2	54	RESERVED	---	X	X	Please leave this pin open
J2	55	USB_OTG_ID	USB1_ID	I	3.3V	Input
J2	56	SD_A_RST	SD1_RESET_B	O	3.3V	
J2	57	USB_OTG_DP	USB1_DP	I/O		
J2	58	SD_A_WP	GPIO1_IO07	O	3.3V	
J2	59	USB_OTG_DN	USB1_DN	I/O		
J2	60	SD_A_CD	GPIO1_IO06	I	3.3V	
J2	61	GND		PWR	GND	
J2	62	SD_A_CMD	SD1_CMD	I/O	SD_A_VCC	
J2	63	PWM	SPDIF_EXT_CLK	O	3.3V	
J2	64	SD_A_CLK	SD1_CLK	O	SD_A_VCC	
J2	65	GPIO_J2_65	SAI2_MCLK	I/O	3.3V	*7
J2	66	SD_A_DATA0	SD1_DATA0	I/O	SD_A_VCC	
J2	67	GPIO_J2_67	GPIO1_IO09	I/O	3.3V	*7
J2	68	SD_A_DATA1	SD1_DATA1	I/O	SD_A_VCC	
J2	69	GPIO_J2_69	SAI2_TXC	I/O	3.3V	*7
J2	70	SD_A_DATA2	SD1_DATA2	I/O	SD_A_VCC	
J2	71	GND		PWR	GND	
J2	72	SD_A_DATA3	SD1_DATA3	I/O	SD_A_VCC	
J2	73	GPIO_J2_73	SAI2_TXD0	I/O	3.3V	*7

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	74	SD_A_DATA4	SD1_DATA4	I/O	SD_A_VCC	
J2	75	GPIO_J2_75	SAI3_RXFS	I/O	3.3V	*7
J2	76	SD_A_DATA5	SD1_DATA5	I/O	SD_A_VCC	
J2	77	GPIO_J2_77	SAI1_RXFS	I/O	3.3V	*7
J2	78	SD_A_DATA6	SD1_DATA6	I/O	SD_A_VCC	
J2	79	GPIO_J2_79	SAI1_RXC	I/O	3.3V	*7
J2	80	SD_A_DATA7	SD1_DATA7	I/O	SD_A_VCC	
J2	81	GND		PWR	GND	
J2	82	GND		PWR	GND	
J2	83	SPI_C_SS0	ECSPI2_SS0	O	3.3V	*8
J2	84	SD_B_RST	SD2_RST	O	SD_B_VCC	
J2	85	SPI_C_MISO	ECSPI2_MISO	I	3.3V	*8
J2	86	SD_B_WP	SD2_WP	O	SD_B_VCC	
J2	87	SPI_C_MOSI	ECSPI2_MOSI	O	3.3V	*8
J2	88	SD_B_CD	SD2_CD_B	I	SD_B_VCC	
J2	89	SPI_C_SCLK	ECSPI_SCLK	O	3.3V	*8
J2	90	SD_B_CMD	SD2_CMD	O	SD_B_VCC	
J2	91	GND		PWR	GND	
J2	92	SD_B_CLK	SD2_CLK	O	SD_B_VCC	
J2	93	JTAG_TCK	JTAG_TCK	I	1.8V	
J2	94	SD_B_DATA0	SD2_DATA0	I/O	SD_B_VCC	
J2	95	JTAG_TMS	JTAG_TMS	I	1.8V	
J2	96	SD_B_DATA1	SD2_DATA1	I/O	SD_B_VCC	
J2	97	JTAG_TDI	JTAG_TDI	I	1.8V	
J2	98	SD_B_DATA2	SD2_DATA2	I/O	SD_B_VCC	
J2	99	JTAG_TDO	JTAG_TDO	O	1.8V	
J2	100	SD_B_DATA3	SD2_DATA3	I/O	SD_B_VCC	

Table 2: B2B connector

*1: These pins have optional connections/features. See Chapter 4.13 for the pin connections

*2: These pins have optional connections/features. See Chapter 4.11 for the pin connections

*3: These pins are CPU dependent. See Chapter 4.10 for the pin connections

*4: These pins have optional connections/features. See Chapter 4.8 for the pin connections

*5: These pins have optional connections/features. See Chapter 4.9 for the pin connections

*6: These pins are CPU dependent. See Chapter 4.1 for the pin connections

*7: These pins are optional GPIOs which depends on assembly variation. See Chapter 4.14 for the alternative usages.

*8: These pins have optional connections/features. See Chapter 4.4 for the pin connections

4 Interfaces

4.1 USB OTG & Host

PicoCoreMX8Mx board can support 1x USB HOST Mode and 1x USB OTG.

The 90 Ohm differential pair of USB signals doesn't need any termination.

For external ports ESD and EMV protection is required nearby the USB connectors.

If the USB OTG will be used in Host Mode, contact **USB_OTG_ID** must be connected to GND via a resistor. Otherwise it must be directly connected to the USB connector.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	41	USB_HOST_VBUS*1	USB2_VBUS	I	5.0V	N.C. for USB Host
J2	43	USB_HOST_DP*1	USB2_DP	I/O		90 Ohm differential pair; Preferred for host
J2	45	USB_HOST_DN*1	USB2_DN	I/O		
J2	47	USB_HOST_PWRn*1*2	GPIO1_IO14	O	3.3V	Power enable; onboard pull-up 100k
J2	51	USB_OTG_VBUS	USB1_VBUS	I	5.0V	Input; USB Phy voltage detection
J2	53	USB_OTG_PWRn	GPIO1_IO12	O	3.3V	Power enable; onboard Pull-Up 100k
J2	55	USB_OTG_ID	USB1_ID	I	3.3V	
J2	57	USB_OTG_DP	USB1_DP	I/O		90 Ohm differential pair
J2	59	USB_OTG_DN	USB1_DN	I/O		

Table 3: USB OTG & Host Interface Connections

*1 The modules with i.MX8M Nano processors only have one USB OTG. And the related pins (J2_41, J2_43, J2_45) on the connector are N.C. (USB Host option is not supported.)

*2 USB_HOST_PWRn pin can be used as a standard GPIO on the modules that have i.MX8M Nano processor.

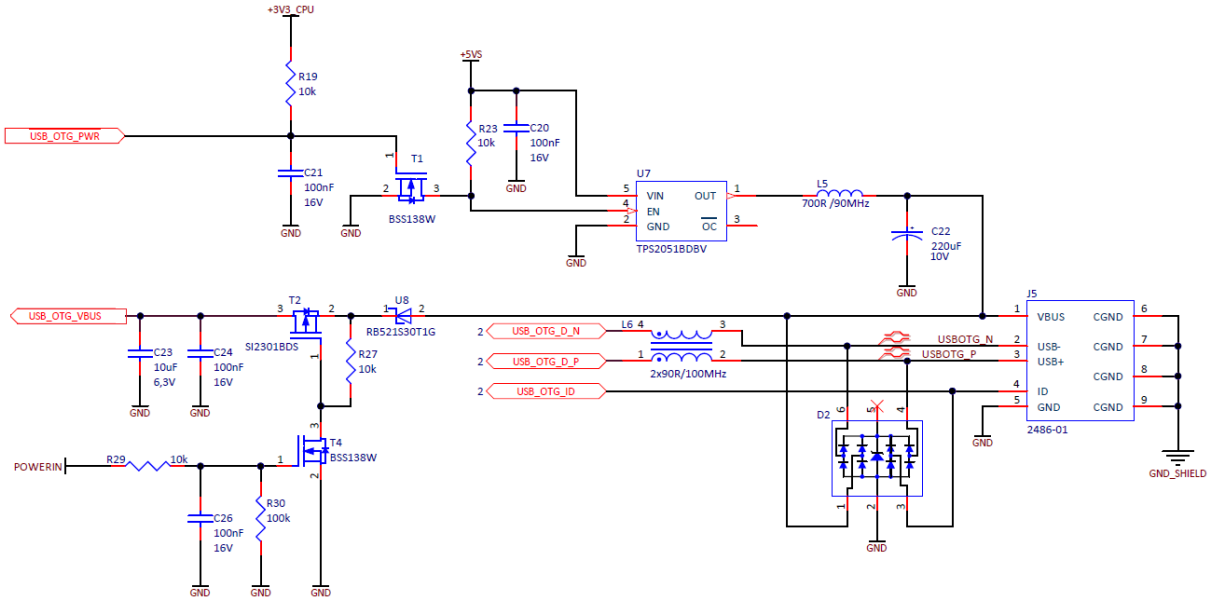

Figure 5: USB OTG example connection

4.2 SD Card Interface A

This interface supports 8bit SD/MMC interface. For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

SD_A_VCC can be 1.8V or 3.3V. The voltage level is configured by the driver.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	52	SD_A_VCC	NVCC_SD1	O	1.8V / 3.3V	Power supply out for external SDIO interface
J2	54	RESERVED	RESERVED	X	X	*1 Do not connect Reserved for future use
J2	56	SD_A_RST	SD1_RESET_B	O	SD_A_VCC	
J2	58	SD_A_WP	GPIO1_IO07	I	3.3V	Active low write protect disable onboard Pull-up 10k
J2	60	SD_A_CD	GPIO1_IO06	I	3.3V	Active low card detect onboard Pull-up 10k
J2	62	SD_A_CMD	SD1_CMD	O	SD_A_VCC	onboard Pull-Up 100k
J2	64	SD_A_CLK	SD1_CLK	O	SD_A_VCC	
J2	66	SD_A_DATA0	SD1_DATA0	I/O	SD_A_VCC	onboard Pull-Up 100k
J2	68	SD_A_DATA1	SD1_DATA1	I/O	SD_A_VCC	
J2	70	SD_A_DATA2	SD1_DATA2	I/O	SD_A_VCC	
J2	72	SD_A_DATA3	SD1_DATA3	I/O	SD_A_VCC	
J2	74	SD_A_DATA4	SD1_DATA4	I/O	SD_A_VCC	
J2	76	SD_A_DATA5	SD1_DATA5	I/O	SD_A_VCC	
J2	78	SD_A_DATA6	SD1_DATA6	I/O	SD_A_VCC	
J2	80	SD_A_DATA7	SD1_DATA7	I/O	SD_A_VCC	

Table 4: SD Card Interface A

*1 in previous versions of the documentation this pin was described as SD_A_VSEL. This pin now does not have any functions.

4.3 SD Card Interface B

This interface is supporting a 4Bit SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

The supply voltage of SD_B (SD_B_VCC) can be set to 1.8V or 3.3V via mounting option.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	84	SD_B_RST	SD2_RESET_B	O	SD_B_VCC	onboard pull-up 100k
J2	86	SD_B_WP	SD2_WP	I	SD_B_VCC	Active low write protect disable
J2	88	SD_B_CD	SD2_CD_B	I	SD_B_VCC	Active low card detect
J2	90	SD_B_CMD	SD2_CMD	I/O	SD_B_VCC	Command/Response, onboard pull-up 100k
J2	92	SD_B_CLK	SD2_CLK	O	SD_B_VCC	
J2	94	SD_B_DATA0	SD2_DATA0	I/O	SD_B_VCC	onboard pull-up 100k
J2	96	SD_B_DATA1	SD2_DATA1	I/O	SD_B_VCC	
J2	98	SD_B_DATA2	SD2_DATA2	I/O	SD_B_VCC	
J2	100	SD_B_DATA3	SD2_DATA3	I/O	SD_B_VCC	

Table 5: SD Card Interface

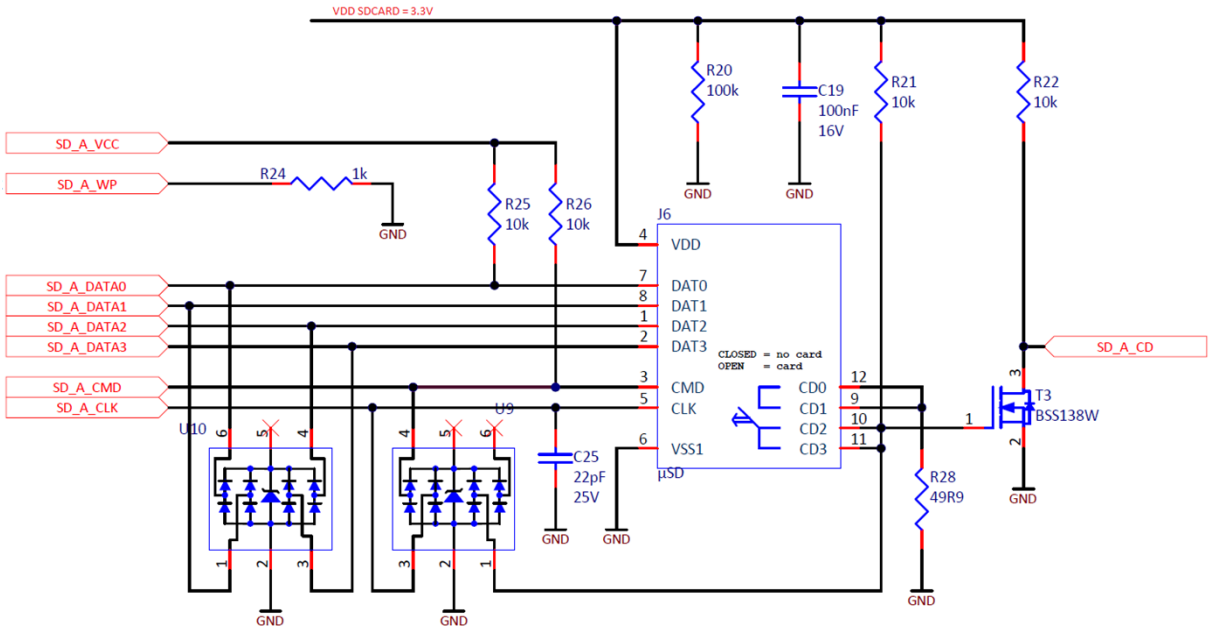

Figure 6: SD Card Connector example connection

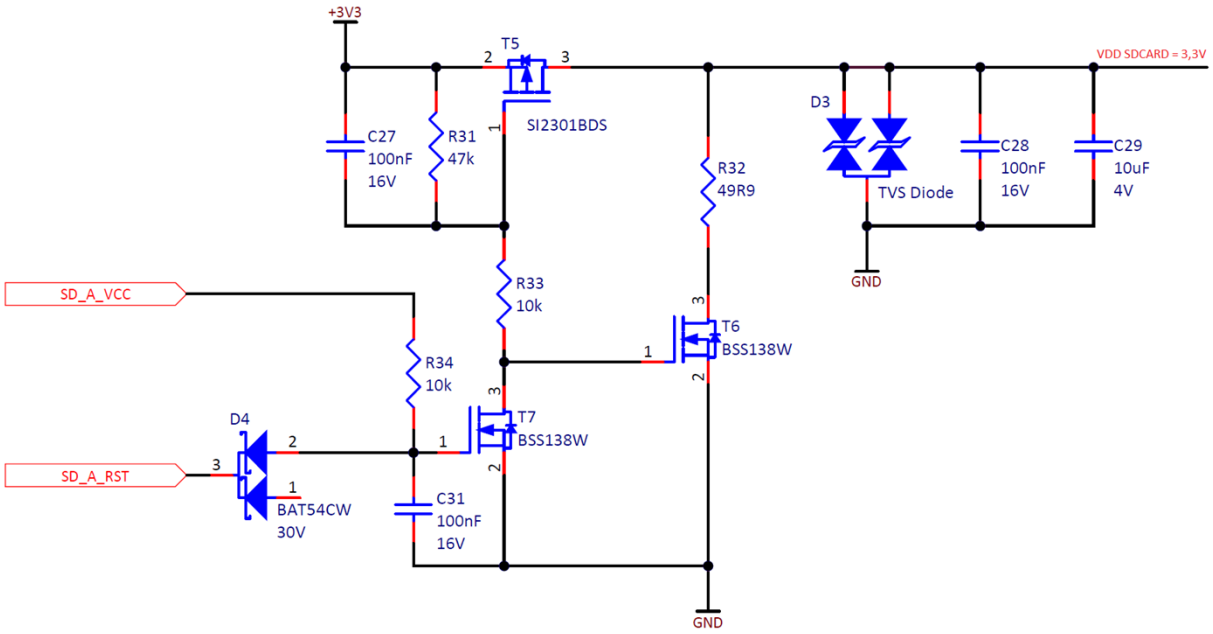

Figure 7: SD_A supply voltage switching circuit

4.4 SPI Interface

The module support Hi-Speed SPI (Serial Peripheral Interface). All signals are 3.3V compliant. Devices on baseboard with other voltage levels need a level shifter.

Signals don't have pull-ups on module.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	SM*2	MM*2	Voltage	Remarks
SPI_A							
J1	64	SPI_A_SS0	ECSPI1_SS0	I	O	3.3V	
J1	66	SPI_A_MISO	ECSPI1_MISO	O	I	3.3V	
J1	68	SPI_A_MOSI	ECSPI1_MOSI	I	O	3.3V	
J1	70	SPI_A_SCLK	ECSPI1_SCLK	I	O	3.3V	
SPI_B							
J1	56	SPI_B_SS0*3	UART1_RXD	I	O	3.3V	ECSPI3_SS0
J1	58	SPI_B_MISO*3	UART1_TXD	O	I	3.3V	ECSPI3_MISO
J1	60	SPI_B_MOSI*3	UART2_RXD	I	O	3.3V	ECSPI3_MOSI
J1	62	SPI_B_SCLK*3	UART2_TXD	I	O	3.3V	ECSPI3_SCLK
SPI_C*1 (without CAN FD)							
J2	83	SPI_C_SS0*1	ECSPI2_SS0	I	O	3.3V	Optional
J2	85	SPI_C_MISO*1	ECSPI2_MISO	O	I	3.3V	Optional
J2	87	SPI_C_MOSI*1	ECSPI2_MOSI	I	O	3.3V	Optional
J2	89	SPI_C_SCLK*1	ECSPI2_SCLK	I	O	3.3V	Optional
SPI_C*1 (with CAN FD)							
J2	83	SPI_C_SS0*1	N.C.				
J2	85	SPI_C_MISO*1	N.C.				
J2	87	SPI_C_MOSI*1	N.C.				
J2	89	SPI_C_SCLK*1	N.C.				

Table 6: SPI Interface Signals

*1 Optional with CAN FD-Interface (no connection if CAN FD is on board)
*2 SM: PicoCore is Slave; MM: PicoCore is Master
*3 Interface SPI_B is in parallel to the interface QSPI. QSPI is an assembly option. See chapter *4.5*.

4.5 QSPI

The module can support optionally the QSPI interface. This feature comes in start with the HW Revision 1.20. On older versions of module there is no QSPI Interface support. The contacts for the QSPI interface are parallel to the contacts for SPI_B, so they cannot be used at the same time.

QSPI Interface can be available on modules with eMMC Flash. The NAND Flash versions do not have QSPI support.

For the QSPI assembly option please contact to our support team.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	52	GPIO_J1_52	NAND_DATA0	I/O	1.8V	QSPI_DATA0
J1	54	GPIO_J1_54	NAND_DATA1	I/O	1.8V	QSPI_DATA1
J1	56	SPI_B_SS0	NAND_CE0_B	O	1.8V	QSPI_CS0
J1	58	SPI_B_MISO	NAND_DATA2	I/O	1.8V	QSPI_DATA2
J1	60	SPI_B_MOSI	NAND_DATA3	I/O	1.8V	QSPI_DATA3
J1	62	SPI_B_SCLK	NAND_ALE	O	1.8V	QSPI_SCLK

Table 7: QSPI Interface

4.6 I2C

The module supports up to four I2C interfaces. Devices on baseboard with other voltage need a level shifter. It's the preferred I2C for touch controller.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	4	I2C_A_SCL	I2C4_SCL	O	3.3V	onboard pull-up 2.49k
J1	6	I2C_A_SDA	I2C4_SDA	I/O	3.3V	onboard pull-up 2.49k
J1	3	I2C_B_SCL	I2C2_SCL	O	3.3V	onboard pull-up 2.49k
J1	5	I2C_B_SDA	I2C2_SDA	I/O	3.3V	onboard pull-up 2.49k
J1	1	I2C_B_IRQ	SAI3_MCLK	I	3.3V	
J1	40	I2C_C_SCL	I2C3_SCL	O	3.3V	onboard pull-up 2.49k
J1	42	I2C_C_SDA	I2C3_SDA	I/O	3.3V	onboard pull-up 2.49k
J1	48	I2C_D_SCL	I2C1_SCL	O	3.3V	onboard pull-up 2.49k
J1	50	I2C_D_SDA	I2C1_SDA	I/O	3.3V	onboard pull-up 2.49k

Table 8: I2C Interface Signals

Note: I2C_D is used on the module to control several devices (i.e. PMIC, RTC, Audio Codec, …). Therefore it's not possible to use this contacts as GPIO or any other function. For I2C_D, PicoCore is always the bus master. Please use I2C_A/B/C before using I2C_D.

4.7 Serial Interfaces (UART)

PicoCoreMX8Mx module provides 4 UART channels (2x UART with flow control signals RTS and CTS, 2x standard RX and TX).

We recommend to use UART_A for debugging and service only.

F&S standard software uses DCE mode for UART.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	14	UART_A_RTS	SAI2_TXFS	O	3.3V	Reserved for debug
J1	16	UART_A_CTS	SAI2_RXD0	I	3.3V	Reserved for debug
J1	18	UART_A_RXD	SAI2_RXC	I	3.3V	Reserved for debug, onboard pull-up 100k
J1	20	UART_A_TXD	SAI2_RXFS	O	3.3V	Reserved for debug
J1	22	UART_B_RTS	SAI3_RXC	O	3.3V	
J1	24	UART_B_CTS	SAI3_RXD	I	3.3V	
J1	26	UART_B_RXD	SAI3_TXFS	I	3.3V	onboard pull-up 100k
J1	28	UART_B_TXD	SAI3_TXC	O	3.3V	
J1	30	UART_C_RXD	UART4_RXD	I	3.3V	onboard pull-up 100k
J1	32	UART_C_TXD	UART4_TXD	O	3.3V	
J1	34	UART_D_RXD	UART3_RXD	I	3.3V	onboard pull-up 100k
J1	36	UART_D_TXD	UART3_TXD	O	3.3V	

Table 9: UART A/B/C/D Interface Signals

4.8 Ethernet

On the PicoCoreMX8Mx module there are two options for the Ethernet interface. There is an assembly option to select between RGMII interface or 2x Gbit LAN.

4.8.1 Ethernet RGMII Interface

Without Ethernet Switch: The module supports one 10/100/1000Mbit LAN interface via RGMII signals. The RGMII signals can be reached from the B2B Connector. An external Ethernet-Phy (i.e. AR8035-AL1A) or an external Ethernet switch is required.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	1	ETH_A_D1_P	ENET_MDC	O	3.3V	
J2	3	ETH_A_D1_N	ENET_MDIO	I/O	3.3V	
J2	5	ETH_A_D2_P	RGMII_TX_CTL	O	3.3V	
J2	7	ETH_A_D2_N	RGMII_TXC	O	3.3V	
J2	9	ETH_A_D3_P	RGMII_TXD0	O	3.3V	
J2	11	ETH_A_D3_N	RGMII_TXD1	O	3.3V	
J2	13	ETH_A_D4_P	RGMII_TXD2	O	3.3V	
J2	15	ETH_A_D4_N	RGMII_TXD3	O	3.3V	
J2	23	ETH_B_D1_P	RGMII_RX_CTL	I	3.3V	
J2	25	ETH_B_D1_N	RGMII_RXC_R	I	3.3V	
J2	27	ETH_B_D2_P	RGMII_RXD0	I	3.3V	
J2	29	ETH_B_D2_N	RGMII_RXD1	I	3.3V	
J2	31	ETH_B_D3_P	RGMII_RXD2	I	3.3V	
J2	33	ETH_B_D3_N	RGMII_RXD3	I	3.3V	
J2	35	ETH_B_D4_P	ETH_SW_RST	O	3.3V	Eth Switch/PHY Reset
J2	37	ETH_B_D4_N	ETH_SW_INTn	I	3.3V	Eth Switch/PHY Interrupt, active low

Table 10: Ethernet Interface RGMII Signals (no Ethernet Switch)

4.8.2 Ethernet Interface 2x GBit LAN

With Ethernet Switch: The module can support two 10/100/1000Mbit LAN Interfaces. In this case the module comes with the Microchip KSZ9893R Ethernet Switch.

Ethernet data signals are connected as 100-Ohm differential pairs.

	Pin	Signal	KSZ9893R Pad	I/O	Voltage	Remarks
J2	1	ETH_A_D1_P	TXRX1P_A	I/O	1.2V	Ethernet A Data 1+
J2	3	ETH_A_D1_N	TXRX1M_A	I/O	1.2V	Ethernet A Data 1-
J2	5	ETH_A_D2_P	TXRX1P_B	I/O	1.2V	Ethernet A Data 2+
J2	7	ETH_A_D2_N	TXRX1M_B	I/O	1.2V	Ethernet A Data 2-
J2	9	ETH_A_D3_P	TXRX1P_C	I/O	1.2V	Ethernet A Data 3+
J2	11	ETH_A_D3_N	TXRX1M_C	I/O	1.2V	Ethernet A Data 3-
J2	13	ETH_A_D4_P	TXRX1P_D	I/O	1.2V	Ethernet A Data 4+
J2	15	ETH_A_D4_N	TXRX1M_D	I/O	1.2V	Ethernet A Data 4-
J2	17	ETH_A_LED	LED1_0	O	3.3V	Ethernet A LED indicator
J2	21	ETH_B_LED[*1]	LED2_0	O	3.3V	Ethernet B LED indicator
J2	23	ETH_B_D1_P	TXRX2P_A	I/O	1.2V	Ethernet B Data 1+
J2	25	ETH_B_D1_N	TXRX2M_A	I/O	1.2V	Ethernet B Data 1-
J2	27	ETH_B_D2_P	TXRX2P_B	I/O	1.2V	Ethernet B Data 2+
J2	29	ETH_B_D2_N	TXRX2M_B	I/O	1.2V	Ethernet B Data 2-
J2	31	ETH_B_D3_P	TXRX2P_C	I/O	1.2V	Ethernet B Data 3+
J2	33	ETH_B_D3_N	TXRX2M_C	I/O	1.2V	Ethernet B Data 3-
J2	35	ETH_B_D4_P	TXRX2P_D	I/O	1.2V	Ethernet B Data 4+
J2	37	ETH_B_D4_N	TXRX2M_D	I/O	1.2V	Ethernet B Data 4-

Table 11: 2x Gigabit Ethernet Interface with Ethernet Switch

[*1] ETH_B_LED pin is not functional on PCB revision PicoCoreMX8Mx Rev.1.10 and older versions

This component is optional and not mounted in all configurations. Please contact sales to get more information.

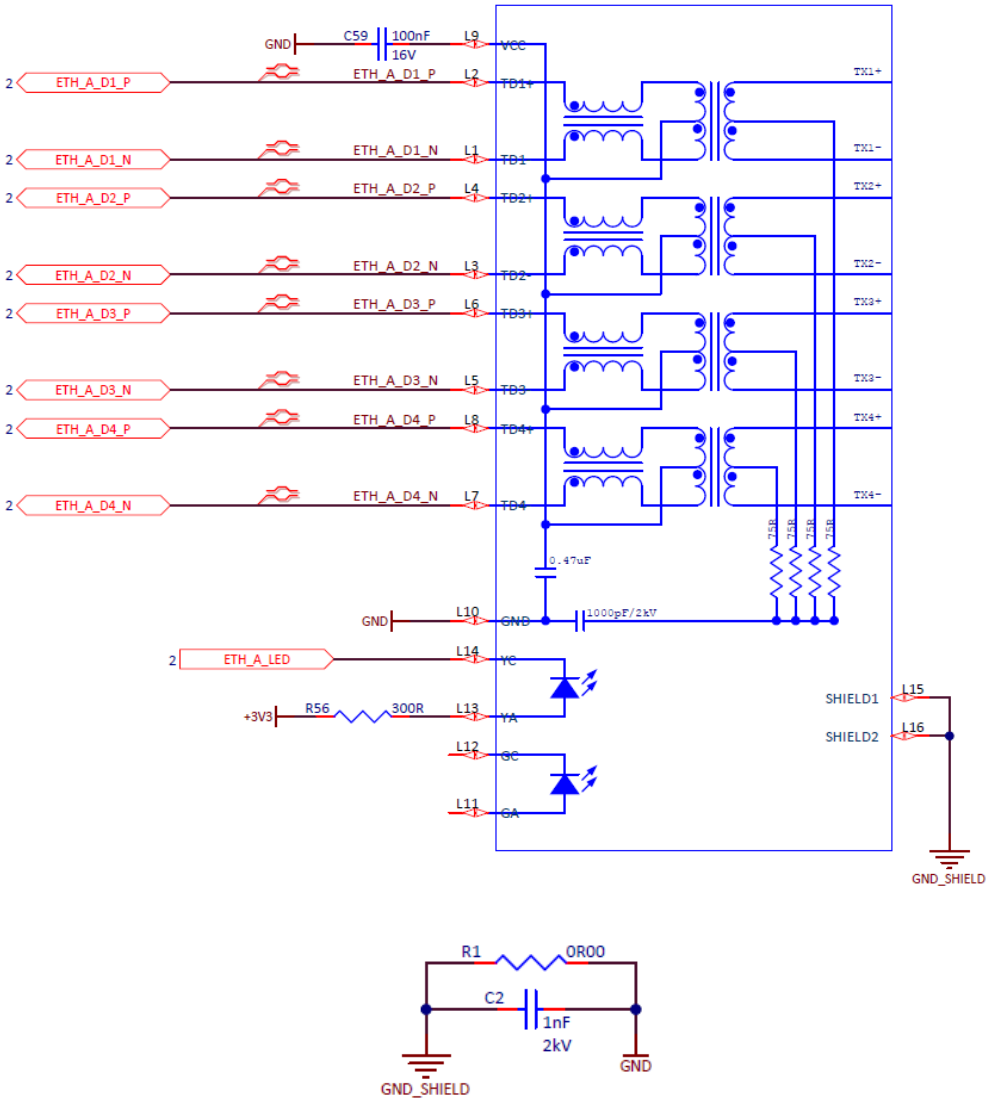

Figure 8: LAN output example

4.9 Audio

The PicoCoreMX8Mx module can support audio interface either directly via I2S signals or with an external audio codec IC. The audio codec NXP SGTL5000 can be mounted on the module optionally. In this case the module can also support the MIC function.

AUDIO_A_VCC is supplied from the PMIC on PicoCore module as default. For a better and smoother audio quality, an external low-noise power supply (e.g. LDO) can be used. AUDIO_A_GND is connected to GND on PicoCore module as default. There is a mounting option to use external GND for the analogue part of the audio codec. Please contact us to have the right assembly option for the external-supplied AUDIO_A_VCC and/or AUDIO_A_GND.

	Pin	Signal	Function	I/O	Voltage	Remarks
J2	2	AUDIO_A_VCC*	VDDA	PWR	3V / 3.3V	Optional: Noise reduced external power supply for audio codec. Default: Onboard connection to 3.3V
J2	4	AUDIO_A_GND	AGND	PWR		Optional: Noise reduced external power supply for audio codec. Default: Onboard connection to GND
J2	6	AUDIO_A_LOUT_L	LOUT	O	AUDIO_A_VCC	
J2	8	AUDIO_A_LOUT_R	ROUT	O	AUDIO_A_VCC	
J2	10	AUDIO_A_MIC	MICIN	I	AUDIO_A_VCC	
J2	12	AUDIO_A_LIN_L	LLINEIN	I	AUDIO_A_VCC	
J2	14	AUDIO_A_LIN_R	RLINEIN	I	AUDIO_A_VCC	
J2	18	AUDIO_A_HP_L	LHPOUT	O	AUDIO_A_VCC	
J2	20	AUDIO_A_HP_R	RHPOUT	O	AUDIO_A_VCC	
J2	22	AUDIO_A_HP_GND	HP_VGND	O		Not connect to common GND directly!

Table 12: Audio Interface (with Audio Codec)

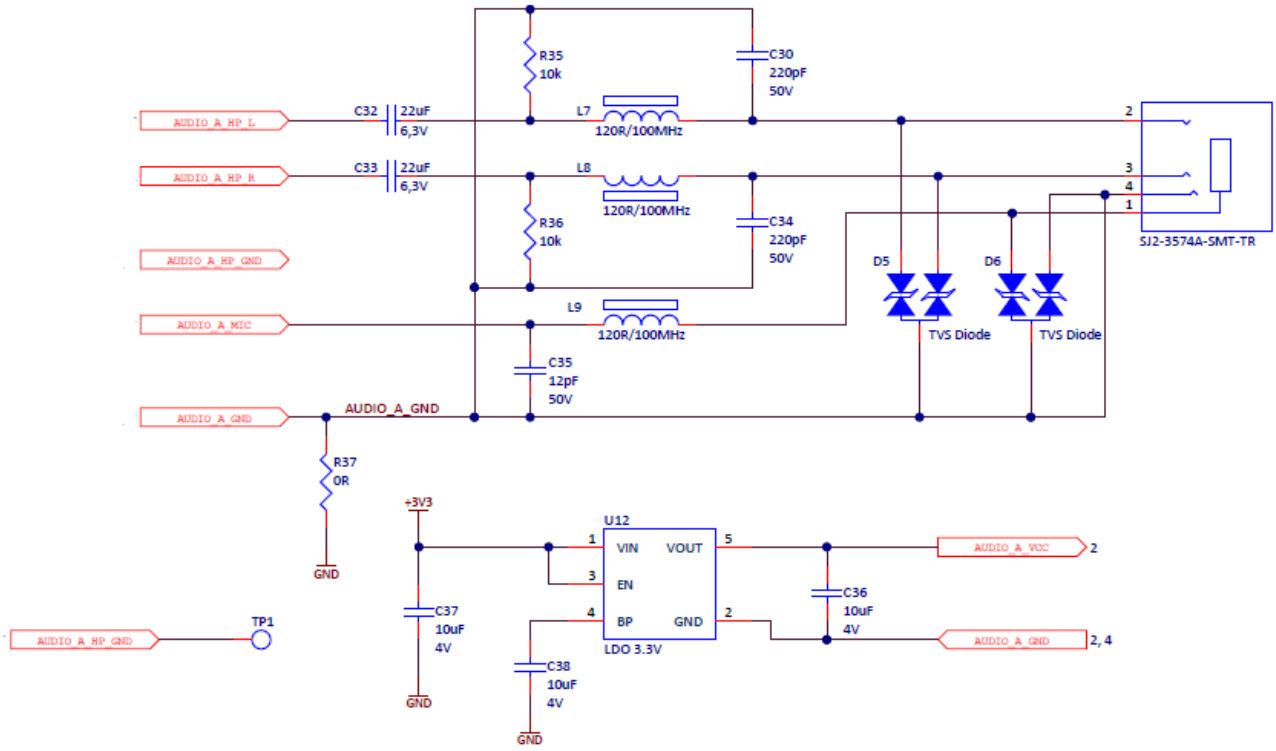

Figure 9: Headphone-Out Mic-In Example Circuit

	Pin	Signal	Function	I/O	Voltage	Remarks
J2	2	AUDIO_A_VCC	N.C.	I	3.3V	Do not connect
J2	4	AUDIO_A_GND	N.C.	I		Do not connect
J2	6	AUDIO_A_LOUT_L	I2S_SCLK	O	3.3V	
J2	8	AUDIO_A_LOUT_R	I2S_LRCLK	O	3.3V	
J2	10	AUDIO_A_MIC	N.C.	X		Do not connect
J2	12	AUDIO_A_LIN_L	I2S_MCLK	O	3.3V	
J2	14	AUDIO_A_LIN_R	N.C.	X		Do not connect
J2	18	AUDIO_A_HP_L	I2S_DOUT	O	3.3V	
J2	20	AUDIO_A_HP_R	I2S_DIN	I	3.3V	
J2	22	AUDIO_A_HP_GND	N.C	X		Do not connect

Table 13: Audio Interface (without Audio Codec)

4.10 PCIE Interface

The PicoCoreMX8Mx module supports single lane PCI Express Gen 2. The interface can work as root complex or endpoint (Dual mode operation).

mPCIe Interface is only supported with i.MX8M Mini based modules.

Modules with i.MX8M Nano do not have mPCIe option and the related pins on the connectors are N.C!

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	77	mPCIE_CTX_P	PCIE_TXN_P	O		PCIe Transmit Data+
J1	79	mPCIE_CTX_N	PCIE_TXN_N	O		PCIe Transmit Data-
J1	83	mPCIE_CRX_P	PCIE_RXN_P	I		PCIe Receive Data+
J1	85	mPCIE_CRX_N	PCIE_TXN_N	I		PCIe Receive Data-
J1	89	mPCIE_CLK_P	PCIE_CLK_P	O		PCIe Clock+
J1	91	mPCIE_CLK_N	PCIE_CLK_N	O		PCIe Clock-
J1	95	mPCIE_PERST	SAI5_RXFS	O		PCIe reset output
J1	97	mPCIE_WAKE	SAI5_RXC	I		PCIe wakeup input

Table 14: PCIE Interface

4.11 MIPI DSI / LVDS Interface

The module supports one quad lane MIPI DSI interface up to 800 Mbps.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	17	DSI_A_CLK_P	MIPI_DSI_CLK_P	O	1.2V/200mV*[1]	
J1	19	DSI_A_CLK_N	MIPI_DSI_CLK_N	O	1.2V/200mV*[1]	
J1	23	DSI_A_DATA0_P	MIPI_DSI_D0_P	O	1.2V/200mV*[1]	
J1	25	DSI_A_DATA0_N	MIPI_DSI_D0_N	O	1.2V/200mV*[1]	
J1	29	DSI_A_DATA1_P	MIPI_DSI_D1_P	O	1.2V/200mV*[1]	
J1	31	DSI_A_DATA1_N	MIPI_DSI_D1_N	O	1.2V/200mV*[1]	
J1	35	DSI_A_DATA2_P	MIPI_DSI_D2_P	O	1.2V/200mV*[1]	
J1	37	DSI_A_DATA2_N	MIPI_DSI_D2_N	O	1.2V/200mV*[1]	
J1	41	DSI_A_DATA3_P	MIPI_DSI_D3_P	O	1.2V/200mV*[1]	
J1	43	DSI_A_DATA3_N	MIPI_DSI_D3_N	O	1.2V/200mV*[1]	
J1	47	DSI_B_CLK_P	N.C.	O		
J1	49	DSI_B_CLK_N	N.C.	O		
J1	53	DSI_B_DATA0_P	N.C.	O		
J1	55	DSI_B_DATA0_N	N.C.	O		
J1	59	DSI_B_DATA1_P	N.C.	O		
J1	61	DSI_B_DATA1_N	N.C.	O		
J1	65	DSI_B_DATA2_P	N.C.	O		
J1	67	DSI_B_DATA2_N	N.C.	O		
J1	71	DSI_B_DATA3_P	N.C.	O		
J1	73	DSI_B_DATA3_N	N.C.	O		

Table 15: MIPI-DSI Interface

*[1]: 1.2V in single-ended mode, approx. 200mV in differential mode

Optional there is a mounting option to get dual channel LVDS (up to 1920x1200 24-bit) instead of MIPI DSI. In this case the module comes with Toshiba TC358775XBG MIPI-DSI to LVDS converter chip.

	Pin	Signal	Function	I/O	Voltage	Remarks
J1	17	DSI_A_CLK_P	LVDS0_CLK_DP	O	1.2V/200mV*1	
J1	19	DSI_A_CLK_N	LVDS0_CLK_DN	O	1.2V/200mV*1	
J1	23	DSI_A_DATA0_P	LVDS0_TX0_DP	O	1.2V/200mV*1	
J1	25	DSI_A_DATA0_N	LVDS0_TX0_DN	O	1.2V/200mV*1	
J1	29	DSI_A_DATA1_P	LVDS0_TX1_DP	O	1.2V/200mV*1	
J1	31	DSI_A_DATA1_N	LVDS0_TX1_DN	O	1.2V/200mV*1	
J1	35	DSI_A_DATA2_P	LVDS0_TX2_DP	O	1.2V/200mV*1	
J1	37	DSI_A_DATA2_N	LVDS0_TX2_DN	O	1.2V/200mV*1	
J1	41	DSI_A_DATA3_P	LVDS0_TX3_DP	O	1.2V/200mV*1	
J1	43	DSI_A_DATA3_N	LVDS0_TX3_DN	O	1.2V/200mV*1	
J1	47	DSI_B_CLK_P	LVDS1_CLK_DP	O	1.2V/200mV*1	
J1	49	DSI_B_CLK_N	LVDS1_CLK_DN	O	1.2V/200mV*1	
J1	53	DSI_B_DATA0_P	LVDS1_TX0_DP	O	1.2V/200mV*1	
J1	55	DSI_B_DATA0_N	LVDS1_TX0_DN	O	1.2V/200mV*1	
J1	59	DSI_B_DATA1_P	LVDS1_TX1_DP	O	1.2V/200mV*1	
J1	61	DSI_B_DATA1_N	LVDS1_TX1_DN	O	1.2V/200mV*1	
J1	65	DSI_B_DATA2_P	LVDS1_TX2_DP	O	1.2V/200mV*1	
J1	67	DSI_B_DATA2_N	LVDS1_TX2_DN	O	1.2V/200mV*1	
J1	71	DSI_B_DATA3_P	LVDS1_TX3_DP	O	1.2V/200mV*1	
J1	73	DSI_B_DATA3_N	LVDS1_TX3_DN	O	1.2V/200mV*1	

Table 16: 2 Channel LVDS Interface

*1 1.2V in single-ended mode, approx. 200mV in differential mode

4.12 MIPI CSI Interface

The module supports quad lane MIPI CSI interface.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	74	CSI_CLK_P	MIPI_CSI_CLK_P	I	1.8V	CSI Input Clock+
J1	76	CSI_CLK_N	MIPI_CSI_CLK_N	I	1.8V	CSI Input Clock-
J1	80	CSI_DATA0_P	MIPI_CSI_D0_P	I	1.8V	CSI Input Data0+
J1	82	CSI_DATA0_N	MIPI_CSI_D0_N	I	1.8V	CSI Input Data0-
J1	86	CSI_DATA1_P	MIPI_CSI_D1_P	I	1.8V	CSI Input Data1+
J1	88	CSI_DATA1_N	MIPI_CSI_D1_N	I	1.8V	CSI Input Data1-
J1	92	CSI_DATA2_P	MIPI_CSI_D2_P	I	1.8V	CSI Input Data2+
J1	94	CSI_DATA2_N	MIPI_CSI_D2_N	I	1.8V	CSI Input Data2-
J1	98	CSI_DATA3_P	MIPI_CSI_D3_P	I	1.8V	CSI Input Data3+
J1	100	CSI_DATA3_N	MIPI_CSI_D3_N	I	1.8V	CSI Input Data3-

Table 17: MIPI CSI Interface

4.13 CAN FD Interface

The module can also support the CAN FD Interface with an optional external controller. If this option is selected, the module comes with MCP2518FD CAN controller IC which uses one of SPI channel (SPI_C). Then just two SPI channels are available instead of three.

	Pin	Signal	Function	I/O	Voltage	Remarks
J1	10	CAN_RX	RXCAN	I	3.3V	
J1	12	CAN_TX	TXCAN	O	3.3V	
J2	65	GPIO_J2_65	CAN_CLKO/SOF	O	3.3V	
J2	69	GPIO_J2_69	CAN_INTn	O	3.3V	Active low interrupt output
J2	73	GPIO_J2_73	CAN_INT0n	I/O	3.3V	RX Interrupt Output (active low) / GPIO
J2	75	GPIO_J2_75	CAN_INT1n	I/O	3.3V	TX Interrupt Output (active low) / GPIO

Table 18: CAN FD Pin Layout

This component is optional and not mounted in all configurations. Please contact sales to get more information.

	Pin	Signal	Function	I/O	Voltage	Remarks
J1	10	CAN_RX	N.C			No Connection
J1	12	CAN_TX	N.C			No Connection
J2	65	GPIO_J2_65	GPIO_J2_65	I/O	3.3V	Standard GPIO
J2	69	GPIO_J2_69	GPIO_J2_69	I/O	3.3V	Standard GPIO
J2	73	GPIO_J2_73	GPIO_J2_73	I/O	3.3V	Standard GPIO
J2	75	GPIO_J2_75	GPIO_J2_75	I/O	3.3V	Standard GPIO

Table 19: B2B Connector Pin Layout without CAN FD

4.14 GPIO

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pull-ups or pull-downs are configurable by software, but they are not available at board start-up. On a non-powered board it's not allowed to have a voltage on GPIO contacts. Also a higher voltage as the announced IO power is not allowed.

Some of the GPIOs are feature optional. The usage and the availability can be changed with the assembly options. Please contact us to have the right assembly option.

If the Ethernet Switch is mounted on the board then GPIO_J1_44 is connected to this IC and cannot be used as free GPIOs. Otherwise can be used as a free GPIO.

If the LVDS Bridge is mounted on the board then GPIO_J1_46, GPIO_J1_52, GPIO_J1_54 are connected to this IC and cannot be used as free GPIOs.

If the CAN FD Transceiver is mounted on the board then GPIO_J2_65, GPIO_J2_69, GPIO_J2_73 and GPIO_J2_75 are connected to this IC and cannot be used as free GPIOs. Otherwise these GPIOs can be used as free GPIOs.

If the Security Chip is mounted on the Board then GPIO_J2_67 is connected to this IC's Enable Pin and cannot be used as free GPIO. Otherwise can be used as free GPIO

GPIO_J2_77 is connected to SAI1_RXFS Pin and can be used as a free GPIO. This pin has no connection on the modules with i.MX8M Nano processor.

GPIO_J2_79 is connected to SAI1_RXC Pin and can be used as a free GPIO. This pin has no connection on the modules with i.MX8M Nano processor.

Alternatively the modules with i.MX8M Mini processor can support a second audio channel via SAI1 pins. There should be no CAN transceiver, security chip and Ethernet switch mounted on the board in order to reach the complete SAI1 channel.

	Pin	Standard	Alternative 1	Alternative 2	Remarks
J1	2	GPIO_J1_2	X	X	Standard 3.3V GPIO
J1	7	GPIO_J1_7	X	X	Standard 3.3V GPIO
J1	44	GPIO_J1_44	ETH_SW_PMEn	X	
J1	46	GPIO_J1_46	LVDS_STBY	X	
J1	52	GPIO_J1_52	LVDS_RST	X	
J1	54	GPIO_J1_54	LVDS_CLK	X	
J2	65	GPIO_J2_65	CAN_CLKO/SOF	SAI1_MCLK[*1]	
J2	67	GPIO_J2_67	SE050_ENA	SAI1_TXFS[*1]	
J2	69	GPIO_J2_69	CAN_INT0n	SAI1_TXC[*1]	
J2	73	GPIO_J2_73	CAN_INT1n	SAI1_TXD0[*1]	
J2	75	GPIO_J2_75	CAN_INTn	SAI1_RXD0[*1]	
J2	77	GPIO_J2_77	X	SAI1_RXFS[*1]	N.C on Nano Processor
J2	79	GPIO_J2_79	X	SAI1_RXC[*1]	N.C on Nano Processor

Table 20: GPIO Interface Options

[*1] SAI1 Pins are just available with i.MX8M Mini Processor

4.15 JTAG

	Pin	Signal	Function	I/O	Voltage	Remarks
J2	93	JTAG_TCK	JTAG_TCK	I	1.8V	
J2	95	JTAG_TMS	JTAG_TMS	I	1.8V	
J2	97	JTAG_TDI	JTAG_TDI	I	1.8V	
J2	99	JTAG_TDO	JTAG_TDO	O	1.8V	

Table 21: JTAG Interface

- For debug only
- Leave unconnected, if you don't use JTAG
- Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU

5 Flash

PicoCoreMX8Mx can be shipped with SLC NAND Flash or MLC eMMC. By default fuses of i.MX8M Mini/Nano are configured so that PicoCore boots from the assembled flash memory.

Please contact support for other boot options.

5.1 NAND Flash

The board implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored two times in flash memory
- Flash data protected by 32 bit ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system

5.2 eMMC

If mounted instead NAND an eMMC v4.41 or higher with 4GB or more is mounted from several manufacturers.

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

5.3 EEPROM

There is also an extra 2kbit 2-wire EEPROM option on the module which is controlled via I2C signals. Standard modules do not come with an EEPROM. Please contact with our engineers for further informations.

This component is optional and not mounted in all configurations. Please contact sales to get more information.

6 RTC

There is optionally an external RTC (NXP PCF85263ATL) mounted on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

This component is optional and not mounted in all configurations. Please contact sales to get more information.

7 Secure Authenticator IC

The secure tamper-resistant authentication IC NXP SE050 offers a strong cryptographic solution intended to be used by device manufacturers to prove the authenticity of their genuine products. It can be used for brand protection, revenue protection, and or customer safety.

For more information visit NXPs web side.

This component is optional and not mounted in all configurations. Please contact sales to get more information.

8 Power and Power Control Contacts

	Pin	Signal	I/O	Description
J2	24 26 28	VDD_VIN	I	Main power supply input please refer chapter 8 **Error! Not a valid bookmark self-reference.**
J2	30 32 34	GND[*6]	I	Main power supply ground input
J2	36	VDD_VBAT[*1]	I	RTC battery input; tie to 3.0V Please refer chapter 8 **Error! Not a valid bookmark self-reference.**
J2	38	RESERVED	X	(formerly VDD_SNVS) Please leave this pin floating (N.C.)
J2	40	VDD_3V3[*3]	O	20mA output from on module DCDC powered from VDD_VIN
J2	52	SD_A_VCC	I	SDHC power output; 3.3V or 1.8V
J2	51	USB_OTG_VBUS	I	USB Phy voltage input; 5V
J2	41	USB_H_VBUS	I	USB Phy voltage input; 5V
J2	42	RESETINN[*4]	I	Power on reset input; 100k Pull-Up to 1.8V
J2	44	PMIC_STBY[*5]	O	Active high for going to SUSPEND state
J2	46	PMIC_ON_REQ	O	Active high for going to RUN state
J2	48	ON_OFF	I	CPU On/Off control pin, can be used with an external button

Table 22: Power and Power Control

[*1] By using a battery for VBAT the regulation rules have to be followed. Please check with your test laboratory. It's possible to use a supercap instead.

[*2] In the previous versions of this document this pin was stated as VDD_SNVS. This pin has no functions and reserved for the further usages in future. **Please leave this pin open (N.C.)!**

[*3] VDD_3V3 is the 3.3V @20mA power supply of the module generated from PMIC and powered from VDD_VIN. Can be used as an "Enable Signal" for the power regulators on baseboard. Please do not use VDD_3V3 pin as a power supply for carrier board.

[*4] RESETINN is a Reset Input for the module. Will just reset the CPU. Button or OC/OD output will restart the CPU. On power fail VDD_VIN has to be switched off and on to avoid latchup effects.

[*5] PMIC_STBY is going to high, if the CPU is going in standby. This allows switch of peripheral functions and save more power. Wakeup needs support by the driver, you have to check.

[*6] The GND contacts which are given in the table above are the power ground contacts for VDD_VIN. For a better EMC performance it is highly recommended to connect all GND contacts to GND on the carrier board (not just the power ground contacts).

9 Electrical characteristic

9.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IO pins	-0.3	OVDD*+0.3	V
Voltage on any IO with VIN off		0.3	V
USB VBUS	-0.3	5.6	V
Maximum power consumption VDD_VBAT at 85°C		0.6	µA
Maximum output current 3.3V		20	mA

Table 23: Absolute Maximum Ratings

9.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Max	Unit
VDD_VIN	Module main power		2.7	5.5	V
VDD_VBAT	RTC power		0.9	5.5	V
USB_OTG_VBUS	USB supply voltage		4.4	5.5	V
OVDD	On module 3.3V from on module PMIC, delayed after VDD_SNVS		3.15	3.45	V
VDD_3V3	3.3V output for power enable on carrier board		OVDD	OVDD	V
V_{ih}	High Level Input Voltage		0.7*OVDD	OVDD	V
V_{il}	Low Level Input Voltage		0	0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15		V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA		0.15	V
I_o	Output current IOs	3.3V		5	mA
I_{VBAT}	Current consumption VBAT	VDD=3.3V T_A = 25°C		0.22*1	µA

Table 24: DC Electrical Characteristics

*1 Low current: typical 0.22 µA at VDD = 3.3 V and Tamb = 25 °C

10 Thermal Specification

Operating Ranges	Min	Typ	Max	Unit
Consumer Range Environment Temperature	0		+70	°C
Industrial Range Environment Temperature	-40		+85	°C

Note 1: Maximum junction temperature of the CPU is 105°C. In this case cooling is a necessity and highly recommended. See also: *Power consumption and cooling*

Note 2: MIPI to LVDS Bridge can support only -30°C to +85°C. This component is not critical for the booting operation.

Note 3: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN12468 (https://www.nxp.com/docs/en/application-note/AN12468.pdf)

11 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

12 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

13 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

14 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **13.8 Watt** (with i.MX8M Mini Processor) and **12.6 Watt** (with i.MX8M Nano Processor). This values are with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **3 Watt to 11 Watt** on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748

- http://www.eetimes.com/document.asp?doc_id=1276750

15 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months

Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months

For longer storage we recommend vacuum dry packs.

16 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.

Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.

Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

17 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags. The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

18 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 10: Matrix Code Sticker

19 Appendix

Important Notice

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20 Content