Hardware Documentation

efus™MX8X
HW Revision 1.10

Version 004
(2021-11-22)

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About This Document

This document describes how to use the efus™MX8X board with mechanical and electrical information. The latest version of this document can be found at:

https://www.fsembedded.com

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
11.07.2019	001	All		-	Initial Version	MD
27.04.2020	002	All	A, M	3.1, 4.7	Addition of connector P/N Number, Changing of LVDS pin layout and signal names	MD
09.07.2021	003	All	M		Changes for Revision 1.10, updated block diagram	MW
29.07.2021	004	All	M	4.2	Updated information about WLAN/BT module	JK
18.11.2021	004	All	M	7	Enhanced information about thermal characteristics	HF

V	Version
A, M, R	Added, Modified, Removed
Au	Author

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1 Block Diagram

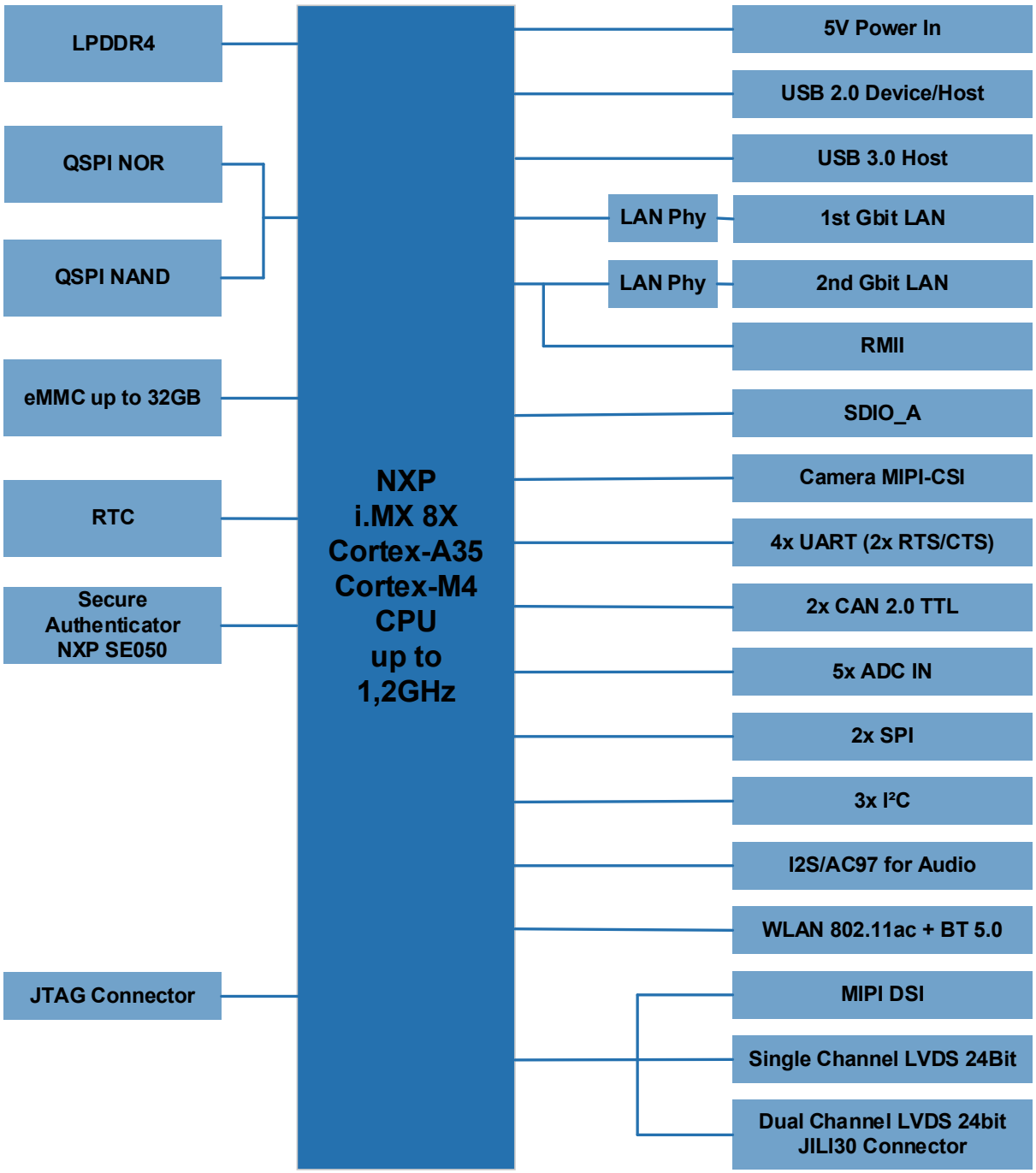

Figure 1: efusMX8X block diagram

2 Mechanical Dimensions

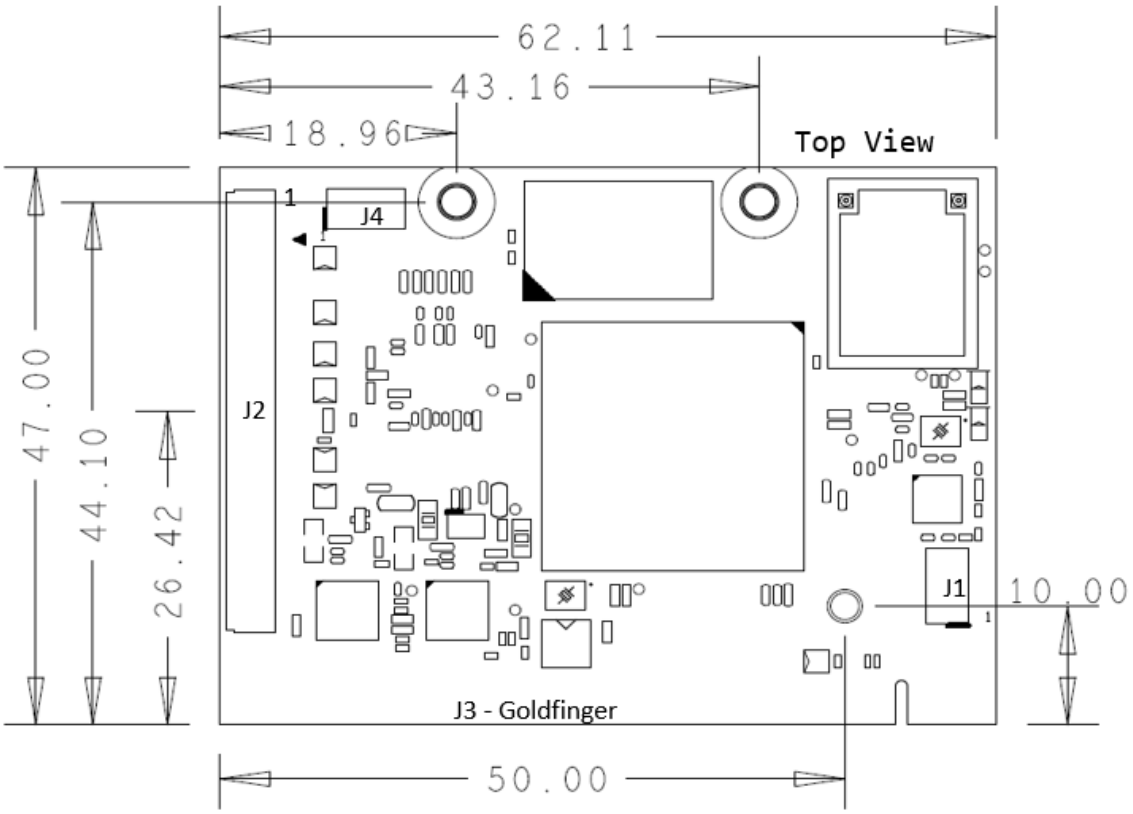

Figure 2: Mechanical Dimensions [mm]

Dimensions	Description
Size	62.1mm x 47mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	4.65mm
Height of the parts on the bottom side	0.9mm
Weight	16gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

3 Interface and Signal Description

3.1 B2B Connector (J3)

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Voltage	Remarks
1	+5V	V5.0	PWR I	5.0V	Power Supply Input
2	+5V	V5.0	PWR I	5.0V	Power Supply Input
3	+5V	V5.0	PWR I	5.0V	Power Supply Input
4	+5V	V5.0	PWR I	5.0V	Power Supply Input
5	+5V	V5.0	PWR I	5.0V	Power Supply Input
6	+5V	V5.0	PWR I	5.0V	Power Supply Input
7	GND	GND	PWR	GND	
8	GND	GND	PWR	GND	
9	VBAT	VBAT	PWR I	3.0V	2.2 < VBAT < 3.45V
10	V33OUT/V33-ENABLE	V3.3	PWR O	3.3V	Max. 20mA output
11	ACOK	NC	X	X	
12	!RESET_IN	RESET_IN	I		
13	I0OUT_ADC_IN	NC	X	X	
14	!RESET_OUT	RESET_OUT	O	3.3V	
15	RXD_C_TTL	UART1_RX	O	3.3V	UART1_RXD
16	SD_A_WP	USDHC1_WP	I	3.3V	
17	TXD_C_TTL	UART1_TX	I	3.3V	UART1_TXD
18	SD_A_CD	USDHC1_CD	I	3.3V	
19	RTS_C_TTL	UART1_RTS_B	O	3.3V	UART1_RTS
20	SD_A_DAT2	USDHC1_D2	I/O	3.3V/1.8V	
21	CTS_C_TTL	UART1_CTS_B	I	3.3V	UART1_CTS
22	SD_A_DAT3	USDHC1_D3	I/O	3.3V/1.8V	
23	PWMB	MIPI_DSI0_GPIO0_00	O	3.3V	ADMA_I2C2_SCL*[1] (optional)
24	USDHC1_CMD	SD_A_CMD	I/O	3.3V/1.8V	
25	PWMA	MIPI_DSI1_GPIO0_00	O	3.3V	MIPI_DSI0_PWM0*[1] (optional)
26	SD_A_VCC	VCC_LDO_SD1	PWR I	3.3V/1.8V	
27	GND	GND	PWR	GND	
28	SD_A_CLK	USDHC1_CLK	O	3.3V/1.8V	
29	CAN_A_TX	FLEXCAN1_TX	O	3.3V	

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Voltage	Remarks
30	GND	GND	PWR	GND	
31	CAN_A_RX	FLEXCAN1_RX	I	3.3V	
32	SD_A_DAT0	USDHC1_D0	I/O	3.3V/1.8V	
33	GND	GND	PWR	GND	
34	SD_A_DAT1	USDHC1_D1	I/O	3.3V/1.8V	
35	CAN_B_TX	FLEXCAN2_TX	O	3.3V	
36	RESERVED1	ADC_IN0	X	1.8V	Optional pins (standard NC)
37	CAN_B_RX	FLEXCAN2_RX	I	3.3V	
38	RESERVED2	ADC_IN1	X	1.8V	Optional pins (standard NC)
39	GND	GND	PWR	GND	
40	RESERVED3	ADC_IN2	X	1.8V	Optional pins (standard NC)
41	MPCIE_CTX_P	NC	X	X	
42	RESERVED4	ADC_IN3	X	1.8V	Optional pins (standard NC)
43	MPCIE_CTX_N	NC	X	X	
44	RESERVED5	ADC_IN4	X	1.8V	Optional pins (standard NC)
45	GND	GND	PWR	GND	
46	GND	GND	PWR	GND	
47	MPCIE_CRX_P	NC	X	X	
48	EXT_PROG	EXT_PROG	I	1.8V	Pulled up to 1.8V with 10K
49	MPCIE_CRX_N	NC	X	X	
50	SPI_B_MISO	SPI3_SDI	I	3.3V	
51	GND	GND	PWR	GND	
52	SPI_B_MOSI	SPI3_SDO	O	3.3V	
53	MPCIE_CLK_P	NC	X	X	
54	SPI_B_SPCK	SPI3_SCK	O	3.3V	
55	MPCIE_CLK_N	NC	X	X	
56	SPI_B_CS1	SPI3_CS0	O	3.3V	
57	GND	GND	PWR	GND	
58	SPI_B_CS2	SPI3_CS1 / MIPI_DSI1_I2C0_SCL	O	3.3V	LSIO_GPIO1_IO29
59	MPCIE_PERST	NC	X	X	
60	SPI_B_IRQ1	CSI_PCLK	I/O	3.3V	LSIO_GPIO3_IO0
61	MPCIE_WAKE	NC	X	X	
62	SPI_B_IRQ2	QSPI0A_DQS	I/O	3.3V	LSIO_GPIO3_IO13

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Voltage	Remarks
63	GND	GND	PWR	GND	
64	GND	GND	PWR	GND	
65	SD_B_DAT2	NC	X	X	
66	SPI_A_MISO	SPI0_SDI	I	3.3V	
67	SD_B_DAT3	NC	X	X	
68	SPI_A_MOSI	SPI0_SDO	O	3.3V	
69	SD_B_CMD	NC	X	X	
70	SPI_A_SPCK	SPI0_SCK	O	3.3V	
71	SD_B_VCC	NC	X	X	
72	SPI_A_CS1	SPI0_CS0	O	3.3V	
73	SD_B_CLK	NC	X	X	
74	SPI_A_CS2	SPI0_CS1	O	3.3V	
75	GND	GND	PWR	GND	
76	SPI_A_IRQ1	SAI1_RXFS	I/O	3.3V	LSIO_GPIO0_IO31
77	SD_B_DAT0	NC	X	X	
78	SPI_A_IRQ2	CSI_MCLK	I/O	3.3V	LSIO_GPIO3_IO1
79	SD_B_DAT1	NC	X	X	
80	GND	GND	PWR	GND	
81	SD_B_WP	NC	X	X	
82	I2C_B_DAT	MIPI_DSI1_GPIO0_01	I/O	3.3V	ADMA_I2C2_SDA (PWMB)*[1]
83	SD_B_CD	NC	X	X	
84	I2C_B_CLK	MIPI_DSI1_GPIO0_00	O	3.3V	ADMA_I2C2_SCL
85	GND	GND	PWR	GND	
86	I2C_B_IRQ	USDHC1_RESET_B	I/O	3.3V	LSIO_GPIO4_IO19
87	BL_CTRL	MIPI_DSI0_GPIO0_00	O	3.3V	MIPI_DSI0_PWM0 (PWMA)*[1]
88	I2C_B_RST	SPI2_SCK	I/O	3.3V	LSIO_GPIO1_IO3
89	VCFL_ON	QSPI0B_SS1_B	I/O	3.3V	LSIO_GPIO3_IO24
90	GND	GND	PWR	GND	
91	GND	GND	PWR	GND	
92	RXD_A_TTL	UART2_RX	I	3.3V	UART2_RXD
93	LCD_CLK	NC	X	X	
94	TXD_A_TTL	UART2_TX	O	3.3V	UART2_TXD
95	GND	GND	PWR	GND	

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Voltage	Remarks
96	RXD_D_TTL	SCU_GPIO0_00	I	3.3V	UART3_RXD
97	LCD_HSYNC	NC	X	X	
98	TXD_D_TTL	SCU_GPIO0_01	O	3.3V	UART3_TXD
99	LCD_VSYNC	NC	X	X	
100	GND	GND	PWR	GND	
101	GND	GND	PWR	GND	
102	RXD_B_TTL	UART0_RX	I	3.3V	UART0_RXD
103	LCD_R0	QSPI0A_SS1_B	I/O	3.3V	LSIO_GPIO3_IO15
104	TXD_B_TTL	UART0_TX	O	3.3V	UART0_TXD
105	LCD_R1	QSPI0B_DQS	I/O	3.3V	LSIO_GPIO3_IO22
106	RTS_B_TTL	FLEXCAN0_RX	O	3.3V	UART0_RTS
107	LCD_R2	MIPI_DSI0_DATA2_P	O	1.8V	LVDSD_H_TX2_P*2*3
108	CTS_B_TTL	FLEXCAN0_TX	I	3.3V	UART0_CTS
109	LCD_R3	MIPI_DSI0_DATA2_N	O	1.8V	LVDSD_H_TX2_N*2*3
110	GND	GND	PWR	GND	
111	LCD_R4	MIPI_DSI0_DATA1_P	O	1.8V	LVDSD_H_TX1_P*2*3
112	I2S_MCLK		O	3.3V	MCLK_OUT0
113	LCD_R5	MIPI_DSI0_DATA1_N	O	1.8V	LVDSD_H_TX1_N*2*3
114	GND	GND	PWR	GND	
115	GND	GND	PWR	GND	
116	I2S_LRCLK	SAI0_TXFS	O	3.3V	
117	LCD_G0	MIPI_DSI0_DATA0_P	O	1.8V	LVDSD_H_TX0_P*2*3
118	GND	GND	PWR	GND	
119	LCD_G1	MIPI_DSI0_DATA0_N	O	1.8V	LVDSD_H_TX0_N*2*3
120	I2S_SCLK	SAI0_TXC	O	3.3V	
121	LCD_G2	MIPI_DSI0_CLK_P	O	1.8V	LVDSD_H_CLK_P*2*3
122	GND	GND	PWR	GND	
123	LCD_G3	MIPI_DSI0_CLK_N	O	1.8V	LVDSD_H_CLK_N*2*3
124	I2S_DOUT	SAI0_TXD	O	3.3V	
125	LCD_G4	MIPI_DSI0_DATA3_P	O	1.8V	LVDSD_H_TX3_P*2*3
126	I2S_DIN	SAI0_RXD	I	3.3V	
127	LCD_G5	MIPI_DSI0_DATA3_N	O	1.8V	LVDSD_H_TX3_N*2*3
128	GND	GND	PWR	GND	

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Voltage	Remarks
129	GND	GND	PWR	GND	
130	I2C_C_DAT	CSI_EN	I/O	3.3V	ADMA_I2C3_SDA
131	LCD_B0	NC	X	X	
132	I2C_C_CLK	CSI_RESET	O	3.3V	ADMA_I2C3_CLK
133	LCD_B1	NC	X	X	
134	HDMI_DDC_VOUT	V3.3	PWR O	3.3V	
135	LCD_B2	NC	X	X	
136	GND	GND	PWR	GND	
137	LCD_B3	NC	X	X	
138	LVDS/DSI_DATA2_P	MIPI_DSI1_DATA2_P	O	1.8V	LVDSC_H_TX2_P*2
139	LCD_B4	NC	X	X	
140	LVDS/DSI _DATA2_N	MIPI_DSI1_DATA2_N	O	1.8V	LVDSC_H_TX2_N*2
141	LCD_B5	NC	X	X	
142	LVDS/DSI _DATA1_P	MIPI_DSI1_DATA1_P	O	1.8V	LVDSC_H_TX1_P*2
143	GND	GND	PWR	GND	
144	LVDS/DSI _DATA1_N	MIPI_DSI1_DATA1_N	O	1.8V	LVDSC_H_TX1_N*2
145	LCD_DE	NC	X	X	
146	LVDS/DSI _DATA0_P	MIPI_DSI1_DATA0_P	O	1.8V	LVDSC_H_TX0_P*2
147	GND	GND	PWR	GND	
148	LVDS/DSI _DATA0_N	MIPI_DSI1_DATA0_N	O	1.8V	LVDSC_H_TX0_N*2
149	VLCD_ON	MIPI_DSI_I2C0_SDA	O	3.3V	
150	LVDS/DSI _CLK_P	MIPI_DSI1_CLK_P	O	1.8V	LVDSC_H_CLK_P*2
151	I2C_A_DAT	USB_SS3_TC3	I/O	3.3V	ADMA_I2C1_SDA | Pulled up to V3.3 with 2.49K
152	LVDS/DSI _CLK_N	MIPI_DSI1_CLK_N	O	1.8V	LVDSC_H_CLK_N*2
153	I2C_A_IRQ	SPI2_SDI	I/O	3.3V	LSIO_GPIO1_IO2
154	LVDS/DSI _DATA3_P	MIPI_DSI1_DATA3_P	O	1.8V	LVDSC_H_TX3_P*2*3
155	I2C_A_CLK	USB_SS3_TC1	O	3.3V	ADMA_I2C1_SCL | Pulled up to V3.3 with 2.49K
156	LVDS/DSI _DATA3_N	MIPI_DSI1_DATA3_N	O	1.8V	LVDSC_H_TX3_N*2*3
157	I2C_A_RST	SPI2_SDO	I/O	3.3V	LSIO_GPIO1_IO1
158	HDMI_HPD	NC	X	X	
159	GND	GND	PWR	GND	
160	GND	GND	PWR	GND	

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Voltage	Remarks
161	CAMINT_YDATA0/D0_N	MIPI_CSI0_DATA0_N	O	1.8V	
162	ETH_B_D4-	-	I/O		ETH2_D_M (AR8035_2) *4
163	CAMINT_YDATA1/D0_P	MIPI_CSI0_DATA0_P	O	1.8V	
164	ETH_B_D4+	-	I/O		ETH2_D_M (AR8035_2) *4
165	CAMINT_YDATA4/D1_N	MIPI_CSI0_DATA1_N	O	1.8V	
166	ETH_B_LED_ACT	-	O	3.3V	ACTLED (AR8035_2) *4
167	CAMINT_YDATA3/D1_P	MIPI_CSI0_DATA1_P	O	1.8V	
168	ETH_B_D3-	-	I/O		ETH2_C_M (AR8035_2) *4
169	CAMINT_YDATA5/D2_N	MIPI_CSI0_DATA2_N	O	1.8V	
170	ETH_B_D3+	-	I/O		ETH2_C_P (AR8035_2) *4
171	CAMINT_YDATA2/D2_P	MIPI_CSI0_DATA2_P	O	1.8V	
172	GND	GND	PWR	GND	
173	CAMINT_YDATA6/D3_N	MIPI_CSI0_DATA3_N	O	1.8V	
174	ETH_B_D2-	-	I/O		ETH2_B_M (AR8035_2) *4
175	CAMINT_PCLK/D3_P	MIPI_CSI0_DATA3_P	O	1.8V	
176	ETH_B_D2+	-	I/O		ETH2_B_P (AR8035_2) *4
177	CAMINT_YDATA7/CLK_N	MIPI_CSI0_CLK_N	O	1.8V	
178	ETH_B_LED_LINK	-	I	3.3V	LINKLED1000 (AR8035_2) *4
179	CAMINT_YDATA8/CLK_P	MIPI_CSI0_CLK_P	O	1.8V	
180	ETH_B_D1-	-	I/O		ETH2_A_M (AR8035_2) *4
181	GND	GND	PWR	GND	
182	ETH_B_D1+	-	I/O		ETH2_A_P (AR8035_2) *4
183	CAMINT_MCLK	MIPI_CSI0_MCLK_OUT_1V8	O	1.8V	
184	GND	GND	PWR	GND	
185	GND	GND	PWR	GND	
186	ETH_CTREF	NC	X	X	
187	CAMINT_YDATA9	NC	X	X	
188	ETH_A_D4-	-	I/O		ETH1_D_M (AR8035_1)
189	CAMINT_VCAM	V1.8	PWR I	1.8V	
190	ETH_A_D4+	-	I/O		ETH1_D_P (AR8035_1)
191	CAMINT_HREF	MIPI_CSI0_I2C0_SCL	O	1.8V	
192	PHY1_LED_ACT	-	O	3.3V	ACTLED (AR8035_1)
193	CAMINT_PWDN	MIPI_CSI0_GPIO0_00	O	1.8V	

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Voltage	Remarks
194	ETH_A_D3-	-	I/O		ETH1_C_M (AR8035_1)
195	CAMINT_VSYNC	MIPI_CSI0_I2C0_SDA	I/O	1.8V	
196	ETH_A_D3+	-	I/O		ETH1_C_P (AR8035_1)
197	I2C_C_CAMRST	MIPI_CSI0_GPIO0_01	I	1.8V	
198	ETH_VLEDOUT	V3.3	PWR O	3.3V	Ethernet LED Output Voltage
199	GND	GND	PWR	GND	
200	ETH_A_D2-	-	I/O		ETH1_B_M (AR8035_1)
201	SATA_RX_P	NC	X	X	
202	ETH_A_D2+	-	I/O		ETH1_B_P (AR8035_1)
203	SATA_RX_N	NC	X	X	
204	ETH_A_LED_LINK	-	I	3.3V	LINKLED1000 (AR8035_1)
205	SATA_TX_N	NC	X	X	
206	ETH_A_D1-	-	I/O		ETH1_A_M (AR8035_1)
207	SATA_TX_P	NC	X	X	
208	ETH_A_D1+	-	I/O		ETH1_A_P (AR8035_1)
209	GND	GND	PWR	GND	
210	GND	GND	PWR	GND	
211	CAM_A_IN	NC	X	X	
212	USB_PWRON	PRTPWR1	O	3.3V	USB_A_PWR
213	CAM_A_GND	NC	X	X	
214	USB_A_N	USBDN1_DM	I/O		USB_A_DN
215	GND	GND	PWR	GND	
216	USB_A_P	USBDN1_DP	I/O		USB_A_DP
217	USB_DEV_VBUS	USB_OTG1_VBUS	PWR I	5.0V	USB_DEV_VBUS
218	GND	GND	PWR	GND	
219	USB_DEV_PWR_ON	USB_SS3_TC0	O	3.3V	USB_DEV_PWR
220	USB_A_SSRX_N	USB_SS3_RX_N	I/O		USB_SS_RX_N
221	USB_DEV_OC	USB_SS3_TC2	I	3.3V	USB_DEV_OC
222	USB_A_SSRX_P	USB_SS3_RX_P	I/O		USB_SS_RX_P
223	USB_DEV_ID	USB_OTG1_ID	I	3.3V	USB_DEV_ID
224	GND	GND	PWR	GND	
225	USB_DEV_N	USB_OTG1_DN	I/O		USB_DEV_DN
226	USB_A_SSTX_N	USB_SS3_TX_N	I/O		USB_SS_TX_N

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Voltage	Remarks
227	USB_DEV_P	USB_OTG1_DP	I/O		USB_DEV_DP
228	USB_A_SSTX_P	USB_SS3_TX_P	I/O		USB_SS_TX_P
229	GND	GND	PWR	GND	
230	GND	GND	PWR	GND	
231	MOUNTINGHOLE_1	NC	X	X	Mounting holes
232	MOUNTINGHOLE_2	NC	X	X	Mounting holes

**1 Optional*

**2 LVDS Signals will be carried to J3 connector only if J2 is not assembled on board*

**3 Comes with HW Rev. 1.10 (NC on older revisions)*

**4 IN HW Rev. 1.10 these pins can be optional RMII. For more information's check Ethernet Section*

Table 2: B2B Connector Pin Layout

4 Interfaces

4.1 Ethernet

On efus™MX8X board by standard there are 2 standard Gigabit Ethernet connections. Optional for iMX8Dual Ethernet 2 is without a Phy and RMII is directly routed to the MXM Connector. We recommend a connector with integrated transformer in short distance (less than 1 inch = 25.4 mm) to the module connector. The RX pair should have a 0.1 inch min. distance to TX pair to avoid crosstalk. The intra pair mismatch of each differential pair should be <10 mil (0.254mm). LED signal is able to drive a 3.3V powered LED with 5mA directly to GND. If Ethernet is not used please leave signals unconnected.

4.1.1 2x GBit Phy

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Description
208	ETH_A_D1+	ETH1_A_P (AR8035_1)	I/O	Ethernet 1 Data Lane 1+
206	ETH_A_D1-	ETH1_A_M (AR8035_1)	I/O	Ethernet 1 Data Lane 1-
202	ETH_A_D2+	ETH1_B_P (AR8035_1)	I/O	Ethernet 1 Data Lane 2+
200	ETH_A_D2-	ETH1_B_M (AR8035_1)	I/O	Ethernet 1 Data Lane 2-
196	ETH_A_D3+	ETH1_C_P (AR8035_1)	I/O	Ethernet 1 Data Lane 3+
194	ETH_A_D3-	ETH1_C_M (AR8035_1)	I/O	Ethernet 1 Data Lane 3-
190	ETH_A_D4+	ETH1_D_P (AR8035_1)	I/O	Ethernet 1 Data Lane 4+
188	ETH_A_D4-	ETH1_D_M (AR8035_1)	I/O	Ethernet 1 Data Lane 4-
192	ETH_A_LED_ACT	ACTLED (AR8035_1)	O	Ethernet 1 Led Action
204	ETH_A_LED_LINK	LEDLINK1000 (AR8035_1)	I	Ethernet 1 Led Link
198	ETH_VLEDOUT	V3.3	PWR O	Ethernet LEDs Supply Voltage
182	ETH_B_D1+	ETH2_A_P (AR8035_2)	I/O	Ethernet 2 Data Lane 1+
180	ETH_B_D1-	ETH2_A_M (AR8035_2)	I/O	Ethernet 2 Data Lane 1-
176	ETH_B_D2+	ETH2_B_P (AR8035_2)	Í/O	Ethernet 2 Data Lane 2+
174	ETH_B_D2-	ETH2_B_M (AR8035_2)	I/O	Ethernet 2 Data Lane 2-
170	ETH_B_D3+	ETH2_C_P (AR8035_2)	I/O	Ethernet 2 Data Lane 3+
168	ETH_B_D3-	ETH2_C_M (AR8035_2)	I/O	Ethernet 2 Data Lane 3-
164	ETH_B_D4+	ETH2_D_P (AR8035_2)	I/O	Ethernet 2 Data Lane 4+
162	ETH_B_D4-	ETH2_D_M (AR8035_2)	I/O	Ethernet 2 Data Lane 4-
166	ETH_B_LED_ACT	ACTLED (AR8035_2)	O	Ethernet 2 Led Action
178	ETH_B_LED_LINK	LINKLED1000(AR8035_2)	I	Ethernet 2 Led Link

Table 3: Ethernet Interface

4.1.2 1x GBit Phy 1x RMII

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Description
208	ETH_A_D1+	ETH1_A_P (AR8035_1)	I/O	Ethernet 1 Data Lane 1+
206	ETH_A_D1-	ETH1_A_M (AR8035_1)	I/O	Ethernet 1 Data Lane 1-
202	ETH_A_D2+	ETH1_B_P (AR8035_1)	I/O	Ethernet 1 Data Lane 2+
200	ETH_A_D2-	ETH1_B_M (AR8035_1)	I/O	Ethernet 1 Data Lane 2-
196	ETH_A_D3+	ETH1_C_P (AR8035_1)	I/O	Ethernet 1 Data Lane 3+
194	ETH_A_D3-	ETH1_C_M (AR8035_1)	I/O	Ethernet 1 Data Lane 3-
190	ETH_A_D4+	ETH1_D_P (AR8035_1)	I/O	Ethernet 1 Data Lane 4+
188	ETH_A_D4-	ETH1_D_M (AR8035_1)	I/O	Ethernet 1 Data Lane 4-
192	ETH_A_LED_ACT	ACTLED (AR8035_1)	O	Ethernet 1 Led Action
204	ETH_A_LED_LINK	LEDLINK1000 (AR8035_1)	I	Ethernet 1 Led Link
198	ETH_VLEDOUT	V3.3	PWR O	Ethernet LEDs Supply Voltage
182	ETH_B_RMII_TXD1	ESAI0_TX5_RX0	I/O	Ethernet 2 Transmit Data0
180	ETH_B_RMII_TX_EN	ESAI0_SCKR	I/O	Ethernet 2 Transmit Enable
176	ETH_B_RMII_TXD0	ESAI0_TX4_RX1	I/O	Ethernet 2 Transmit Data 1
174	ETH_B_RMII_REFCLK	ESAI0_FSR	O	Ethernet 2 Clock Output
170	ETH_B_RMII_RXD0	SPDIF0_RX	I/O	Ethernet 2 Receive Data 0
168	ETH_B_RMII_CRS_DV	SPDIF0_TX	I/O	Ethernet 2 Carrier Sense
164	ETH_B_RMII_RXD1	ESAI0_TX3_RX2	I/O	Ethernet 2 Receive Data 1
162	ETH_B_RMII_RX_ER	ESAI0_TX2_RX3	I/O	Ethernet 2 Receive Error
166	ETH_MDIO	ENET0_MDIO	O	Also used for AR8035 of ETH_A
178	ETH_MDC	ENET0_MDC	I	Also used for AR8035 of ETH_A

Table 4: Ethernet Interface

4.2 WLAN and Bluetooth

The efus™MX8X contains a certified high performance WLAN and Bluetooth module.

The module is based on NXP W8997 chip, having CE, FCC, IC, NCC, AU/NZ, India, Japan pre-certificates.

Please contact support@fs-net.de for additional information about process of certification. The module offers:

- IEEE802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, Bluetooth 3.0 and Bluetooth 5.0 (supports low Energy)

Information about Bluetooth (QDID):

Please refer to the following BT QDID info for 88W8997 (AW-CM276NF).

QDID : D046929

https://launchstudio.bluetooth.com/ListingDetails/91724

If Bluez-5.37 will be used, the QDID from NXP can be used

https://launchstudio.bluetooth.com/ListingDetails/92249

Customer can use this QDIDs to create their device QDID.

Note: PCIe Interface is used for onboard WLAN module and not available for the general customer usage.

4.3 USB

efus™MX8X provides 1x USB3.0 Host only and 1x USBOTG2.0 connections. The 90 Ohm differential pair of USB signals do not need any termination. For external ports EMV and ESD protection is required nearby the USB connector on the base board. If the USB port is not used please leave open.

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Description
212	USB_PWRON	PRTPWR1	I	USB3.0 Host Power On
214	USB_A_N	USBDN1_DM	I/O	USB3.0 Host Data Lane- (in USB2.0 Case)
216	USB_A_P	USBDN1_DP	Í/O	USB3.0 Host Data Lane+ (in USB2.0 Case)
220	USB_A_SSRX_N	USB_SS3_RX_N	I	USB3.0 Host Receive Lane-
222	USB_A_SSRX_P	USB_SS3_RX_P	I/O	USB3.0 Host Receive Lane+
226	USB_A_SSTX_N	USB_SS3_TX_N	I/O	USB3.0 Host Transmit Lane-
228	USB_A_SSTX_P	USB_SS3_TX_P	I/O	USB3.0 Host Transmit Lane+
217	USB_DEV_VBUS	USB_OTG1_VBUS	I/O	USB OTG2.0 Supply Voltage (Input @Device Mode)
219	USB_DEV_PWR_ON	USB_SS3_TC0	I	USB OTG2.0 Power On
221	USB_DEV_OC	USB_SS3_TC2	O	USB OTG2.0 Over Current Output (active low)
223	USB_DEV_ID	USB_OTG1_ID	O	USB OTG2.0 ID
225	USB_DEV_N	USB_OTG1_DN	I/O	USB OTG2.0 Data Lane-
227	USB_DEV_P	USB_OTG1_DP	I/O	USB OTG2.0 Data Lane+

Table 5: USB Interface

4.4 Serial Interfaces

On efus™MX8X board it is allowed for the users to use these serial interfaces, which are given below. All of these serial Interfaces are 3.3V compliant.

- UART: 2 x UART with RTS/CTS and 2 x UART without RTS/CTS
- I2C: 3 x I2C
- SPI: 2 x SPI
- CAN: 2 x CAN Bus

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Description
102	RXD_B_TTL	UART0_RX	I	UART0 Receive Data
104	TXD_B_TTL	UART0_TX	O	UART0 Transmit Data
106	RTS_B_TTL	FLEXCAN0_RX	O	UART0 Request to Send Signal
108	CTS_B_TTL	FLEXCAN0_TX	I	UART0 Clear to Send Signal
15	RXD_C_TTL	UART1_RX	I	UART0 Receive Data
17	TXD_C_TTL	UART1_TX	O	UART0 Transmit Data
19	RTS_C_TTL	UART1_RTS_B	O	UART1 Request to Send Signal
21	CTS_C_TTL	UART1_CTS_B	I	UART1 Clear to Send Signal
92	RXD_A_TTL	UART2_RX	I	UART2 Receive Data
94	TXD_A_TTL	UART2_TX	O	UART2 Transmit Data
96	RXD_D_TTL	SCU_GPIO0_00	I	UART3 Receive Data
98	TXD_D_TTL	SCU_GPIO0_01	O	UART3 Transmit Data

Table 6: Serial Interfaces – UART

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Description
29	CAN_A_TX	FLEXCAN1_TX	O	CAN1 Transmit Data
31	CAN_A_RX	FLEXCAN1_RX	I	CAN1 Receive Data
35	CAN_B_TX	FLEXCAN2_TX	O	CAN2 Transmit Data
37	CAN_B_RX	FLEXCAN2_RX	I	CAN2 Receive Data

**Can transceivers must be placed on Baseboard*

Table 7: Serial Interfaces – CAN

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Description
155	I2C_A_CLK	USB_SS3_TC1	O	I2C1 Clock Lane
151	I2C_A_DAT	USB_SS3_TC3	I/O	I2C1 Data Lane
153	I2C_A_IRQ	SPI2_SDI	I/O	I2C1 Interrupt Signal
157	I2C_A_RST	SPI2_SDO	I	I2C1 Reset Signal
84	I2C_B_CLK	MIPI_DSI1_GPIO0_00	O	I2C2 Clock Lane
82	I2C_B_DAT	MIPI_DSI1_GPIO0_01	I/O	I2C2 Data Lane
86	I2C_B_IRQ	USDHC1_RESET_B	I/O	I2C2 Interrupt Signal
88	I2C_B_RST	SPI2_SCK	I	I2C2 Reset Signal
132	I2C_C_CLK	CSI_RESET	O	I2C3 Clock Lane
130	I2C_C_DAT	CSI_EN	I/O	I2C3 Data Lane

Table 8: Serial Interfaces – I2C

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Description
66	SPI_A_MISO	SPI0_SDI	I	SPI0 Master In Slave Out (Data In)
68	SPI_A_MOSI	SPI0_SDO	O	SPI0 Master Out Slave In (Data Out)
70	SPI_A_SPCK	SPI0_SCK	O	SPI0 Serial Peripheral Clock
72	SPI_A_CS1	SPI0_CS0	O	SPI0 Chip Select 1 (Slave Select 0)
74	SPI_A_CS2	SPI0_CS1	O	SPI0 Chip Select 2 (Slave Select 1)
76	SPI_A_IRQ1	SAI1_RXFS	I/O	SPI0 Interrupt Flag 1 [LSIO_GPIO0_IO31]
78	SPI_A_IRQ2	CSI_MCLK	I/O	SPI0 Interrupt Flag 2 [LSIO_GPIO3_IO1]
50	SPI_B_MISO	SPI3_SDI	I	SPI3 Master In Slave Out (Data In)
52	SPI_B_MOSI	SPI3_SDO	O	SPI3 Master Out Slave In (Data Out)
54	SPI_B_SPCK	SPI3_SCK	O	SPI3 Serial Peripheral Clock
56	SPI_B_CS1	SPI3_CS0	O	SPI3 Chip Select 1 (Slave Select 0)
58	SPI_B_CS2	SPI3_CS1(Rev 1.00) / MIPI_DSI1_I2C0_SCL (Rev 1.10)	O	SPI3 Chip Select 2 (Slave Select 1)
60	SPI_B_IRQ1	CSI_PCLK	I/O	SPI3 Interrupt Flag 1 [LSIO_GPIO3_IO0]
62	SPI_B_IRQ2	QSPI0A_DQS	I/O	SPI3 Interrupt Flag 2 [LSIO_GPIO3_IO13]

There are no pull-up resistors on board

Table 9: Serial Interfaces – SPI

4.5 SD Card

The interface is supporting an SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org. Pullups are not integrated on the module. Unused signals should be left unconnected. SD Interface supply voltage is 3.3V as standard. With the assembly option, 1.8V can also be used.

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Description
32	SD_A_DAT0	USDHC1_DATA0	I/O	SD Card Interface Data Lane 0
34	SD_A_DAT1	USDHC1_DATA1	I/O	SD Card Interface Data Lane 1
20	SD_A_DAT2	USDHC1_DATA2	I/O	SD Card Interface Data Lane 2
22	SD_A_DAT3	USDHC1_DATA3	I/O	SD Card Interface Data Lane 3
24	SD_A_CMD	USDHC1_CMD	I	Command Signal
28	SD_A_CLK	USDHC1_CLK	O	Clock Signal
18	SD_A_CD	USDHC1_CD_B	I	Card Detect Signal
16	SD_A_WP	USDHC1_WP	I	Write Protect Signal
26	SD_A_VCC	V3.3 | VCC_LDO_SD1	PWR I	SD Card Interface Supply Voltage

Table 10: SD Card Interface

4.6 Audio

efus™MX8X board supports SAI Interface (Serial Audio Interface) which is including industry-standard codecs. There are no external audio codecs on this board.

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Description
126	I2S_DIN	SAI0_TXD	I	I2S Data In
124	I2S_DOUT	SAI0_RXD	O	I2S Data Out
116	I2S_LRCLK	SAI0_TXFS	O	I2S Frame Clock
112	I2S_MCLK	MCLK_OUT0	O	I2S System Master Clock
120	I2S_SCLK	SAI0_TXC	O	I2S Bit Clock

Table 11: Audio Interface

4.7 LVDS / MIPI-DSI

efus™MX8X board supports two MIPI-DSI/LVDS Combo PHYs (each up to 1080p60). Each single PHY can either be a 4-lane MIPI-DSI or a 4-lane channel LVDS interface for a total of 2 display interfaces. In combination, the two PHYs can be configured to be a single dual-channel LVDS interface. On efus™MX8X board there is a connector (J2) for the display connection but for single channel usage (LVDSB) it is also possible to use the connections on the B2B connector (J3).

J2 Connector Type: FI-X30SSLA-HF-R2500

Mating Connector (cable side): FI-X30H & FI-X30HL

If the LVDS connector J2 is not assembled on the board, the LVDS signals will be available on the related pins of J3 which is given below at the Table 13. If the J2 is assembled on the board then J3 has HDMI signals as standard instead of LVDS signals. In this case LVDS signals can be reached via J2 connector.

J2 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Description
1	LVDSA_TX0_M	MIPI_DSI0_DATA0_N	O	LVDSA | MIPI_DSI0 Data Lane 0-
2	LVDSA_TX0_P	MIPI_DSI0_DATA0_P	O	LVDSA | MIPI_DSI0 Data Lane 0+
3	LVDSA_TX1_M	MIPI_DSI0_DATA1_N	O	LVDSA | MIPI_DSI0 Data Lane 1-
4	LVDSA_TX1_P	MIPI_DSI0_DATA1_P	O	LVDSA | MIPI_DSI0 Data Lane 1+
5	LVDSA_TX2_M	MIPI_DSI0_DATA2_N	O	LVDSA | MIPI_DSI0 Data Lane 2-
6	LVDSA_TX2_P	MIPI_DSI0_DATA2_P	O	LVDSA | MIPI_DSI0 Data Lane 2+
7	GND		PWR	
8	LVDSA_CLK_M	MIPI_DSI0_CLK_N	O	LVDSA | MIPI_DSI0 Clock Signal-
9	LVDSA_CLK_P	MIPI_DSI0_CLK_P	O	LVDSA | MIPI_DSI0 Clock Signal+
10	LVDSA_TX3_M	MIPI_DSI0_DATA3_N	O	LVDSA | MIPI_DSI0 Data Lane 3-
11	LVDSA_TX3_P	MIPI_DSI0_DATA3_P	O	LVDSA | MIPI_DSI0 Data Lane 3+
12	LVDSB_TX0_M	MIPI_DSI1_DATA0_N	O	LVDSB | MIPI_DSI1 Data Lane 0-
13	LVDSB_TX0_P	MIPI_DSI1_DATA0_P	O	LVDSB | MIPI_DSI1 Data Lane 0+
14	GND		PWR	
15	LVDSB_TX1_M	MIPI_DSI1_DATA1_N	O	LVDSB | MIPI_DSI1 Data Lane 1-
16	LVDSB_TX1_P	MIPI_DSI1_DATA1_P	O	LVDSB | MIPI_DSI1 Data Lane 1+
17	GND		PWR	
18	LVDSB_TX2_M	MIPI_DSI1_DATA2_N	O	LVDSB | MIPI_DSI1 Data Lane 2-
19	LVDSB_TX2_P	MIPI_DSI1_DATA2_P	O	LVDSB | MIPI_DSI1 Data Lane 2+
20	LVDSB_CLK_M	MIPI_DSI1_CLK_N	O	LVDSB | MIPI_DSI1 Clock Signal-
21	LVDSB_CLK_P	MIPI_DSI1_CLK_P	O	LVDSB | MIPI_DSI1 Clock Signal+
22	LVDSB_TX3_M	MIPI_DSI1_DATA3_N	O	LVDSB | MIPI_DSI1 Data Lane 3-
23	LVDSB_TX3_P	MIPI_DSI1_DATA3_P	O	LVDSB | MIPI_DSI1 Data Lane 3+
24	GND		PWR	
25	MIPI_DSI0_I2C0_SDA		I/O	I2C Touch Control Serial Data
26	I2C4_IRQ / VLCDON		I/O	VLCD Enable
27	MIPI_DSI0_I2C0_SCL		O	I2C Touch Control Serial Clock
28	VLCD		PWR O	3.3V(default) / 5.0V
29	VLCD		PWR O	3.3V(default) / 5.0V
30	VLCD		PWR O	3.3V(default) / 5.0V

Table 12: J2 Display Connector Pin Layout

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Description
107	LCD_R2	MIPI_DSI0_DATA2_P	O	LVDSD Data Lane 2+*1*2
109	LCD_R3	MIPI_DSI0_DATA2_N	O	LVDSD Data Lane 2-*1*2
111	LCD_R4	MIPI_DSI0_DATA1_P	O	LVDSD Data Lane 1+*1*2
113	LCD_R5	MIPI_DSI0_DATA1_N	O	LVDSD Data Lane 1-*1*2
117	LCD_G0	MIPI_DSI0_DATA0_P	O	LVDSD Data Lane 0+*1*2
119	LCD_G1	MIPI_DSI0_DATA0_N	O	LVDSD Data Lane 0-*1*2
121	LCD_G2	MIPI_DSI0_CLK_P	O	LVDSD Clock Signal+*1*2
123	LCD_G3	MIPI_DSI0_CLK_N	O	LVDSD Clock Signal-*1*2
125	LCD_G4	MIPI_DSI0_DATA3_P	O	LVDSD Data Lane 3+*1*2
127	LCD_G5	MIPI_DSI0_DATA3_N	O	LVDSD Data Lane 3-*1*2
134	V3.3		PWR O	HDMI_DDC_VOUT | LVDS_VOUT
138	HDMI_DATA2_P	MIPI_DSI1_DATA2_P	O	LVDSC Data Lane 2+*3
140	HDMI_DATA2_N	MIPI_DSI1_DATA2_N	O	LVDSC Data Lane 2-*3
142	HDMI_DATA1_P	MIPI_DSI1_DATA1_P	O	LVDSC Data Lane 1+*3
144	HDMI_DATA1_N	MIPI_DSI1_DATA1_N	O	LVDSC Data Lane 1-*3
146	HDMI_DATA0_P	MIPI_DSI1_DATA0_P	O	LVDSC Data Lane 0+*3
148	HDMI_DATA0_N	MIPI_DSI1_DATA0_N	O	LVDSC Data Lane 0-*3
150	HDMI_CLK_P	MIPI_DSI1_CLK_P	O	LVDSC Clock Signal+*3
152	HDMI_CLK_N	MIPI_DSI1_CLK_N	O	LVDSC Clock Signal-*3
154	HDMI_AUXP	MIPI_DSI1_DATA3_P	O	LVDSC Data Lane 3+*1*3
156	HDMI_DDCCEC	MIPI_DSI1_DATA3_N	O	LVDSC Data Lane 3-*1*3

**1 comes with HW Revision 1.10 (NC on older revisions)*

**2 if J2 is assembled → NC, if J2 not assembled → LVDS Signals on the connector*

**3 if J2 is assembled → HDMI Signals, if J2 not assembled → LVDS Signals on the connector*

Table 13: B2B Connector Display Signals Pin Layout

The processor can support only two LVDS channels. LVDSC and LVDSD channels are not discrete channels. These channels are named differently from LVDSA and LVDSB in order to prevent the confusion because of the signal names.

4.8 MIPI-CSI Interface

The board supports quad lane MIPI-CSI Interface.

J3 Pin	Signal Name	i.MX8QuadXPlus Pin	I/O	Description
161	CAMINT_YDATA0/D0_N	MIPI_CSI0_DATA0_N	O	MIPI-CSI Data Lane 0-
163	CAMINT_YDATA1/D0_P	MIPI_CSI0_DATA0_P	O	MIPI-CSI Data Lane 0+
165	CAMINT_YDATA4/D1_N	MIPI_CSI0_DATA1_N	O	MIPI-CSI Data Lane 1-
167	CAMINT_YDATA3/D1_P	MIPI_CSI0_DATA1_P	O	MIPI-CSI Data Lane 1+
169	CAMINT_YDATA5/D2_N	MIPI_CSI0_DATA2_N	O	MIPI-CSI Data Lane 2-
171	CAMINT_YDATA2/D2_P	MIPI_CSI0_DATA2_P	O	MIPI-CSI Data Lane 2+
173	CAMINT_YDATA6/D3_N	MIPI_CSI0_DATA3_N	O	MIPI-CSI Data Lane 3-
175	CAMINT_PCLK/D3_P	MIPI_CSI0_DATA3_P	O	MIPI-CSI Data Lane 3+
177	CAMINT_YDATA7/CLK_N	MIPI_CSI0_CLK_N	O	MIPI-CSI Clock-
179	CAMINT_YDATA8/CLK_P	MIPI_CSI0_CLK_P	O	MIPI-CSI Clock+
183	CAMINT_MCLK	MIPI_CSI0_MCLK_OUT	O	Camera System Master Clock
189	CAMINT_VCAM	V1.8	PWR O	Camera Supply Voltage
191	CAMINT_HREF	MIPI_CSI0_I2C0_SCL	O	Camera Horizontal Ref. Signal
193	CAMINT_PWDN	MIPI_CSI0_GPIO0_00	O	Camera Power Down Signal
195	CAMINT_VSYNC	MIPI_CSI0_I2C0_SDA	I/O	Camera Vertical Sync Signal
197	I2C_C_CAMRST	MIPI_CSI0_GPIO0_01	I	Camera Reset Signal

Table 14: MIPI-CSI Interface

4.9 JTAG

J1 Pin	Signal Name	I/O	Voltage	Description
1	+VDD_SCU_1V8	PWR	1.8V	
2	JTAG_TMS	X	1.8V	JTAG Test Mode Select
3	GND	PWR	GND	
4	JTAG_TCK	X	1.8V	JTAG Test Clock
5	GND	PWR	GND	
6	JTAG_TDO	X	1.8V	JTAG Test Data Out
7	NC	X	X	
8	JTAG_TDI	X	1.8V	JTAG Test Data In
9	GND	PWR	GND	
10	JTAG_SRST	X	1.8V	JTAG System Reset

Table 15: JTAG Interface

- For debug only
- Leave unconnected, if you don’t use JTAG
- Don’t put them in a JTAG chain, because different power sequence and power level could kill the CPU

4.10 Power and Power Control Pins

J3 Pin	Signal Name	I/O	Voltage	Description
1…6	+5V	PWR In	5.0V	Main Power Supply Input Please refer Electrical characteristic (Ch6)
9	VBAT	PWR In	3V	RTC Battery Input, leave open if not used Please refer Electrical characteristic (Ch6)
10	V33OUT / V33_ENABLE	PWR O	3.3V	20mA Output from on module DCDC powered from V5.0
12	!RESET_IN	I	3.3V	Power On Reset Input
26	SD_A_VCC	O	1.8V/3.3V	SD Card Supply Voltage (VCC_LDO_SD1 | V3.3)
134	HDMI_DDC_VOUT	O	3.3V	HDMI/LVDS Supply Voltage
149	VLCD_ON	I	3.3V	LCD Enable
189	CAMINT_VCAM	O	1.8V	Camera Supply Voltage
198	ETH_VLEDOUT	O	3.3V	Ethernet LED Supply Voltage
217	USB_DEV_VBUS	PWR I/O	5.0V	USB (OTG1) Power Supply (Input for Device Mode)
	GND	PWR	GND	Connect all GND pins to a GND plane

Table 16: Power and Power Control Pins

By using a battery for VBAT you have to follow regulation rules. Please check with your test laboratory.

V33OUT/V33_ENABLE is the DCDC power supply of the module powered from V5.0. Use as enable for baseboard power regulators.

!RESET_IN is a Reset Input for the module. Will just reset the CPU.

5 RTC

There is a NXP PCF85263ATL or compatible implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift over the day.

6 Electrical characteristic

6.1 Absolute maximum ratings

Description	Min	Max	Unit
I/O Voltage range for 1.8V IO pins	-0.3	2.1	V
I/O Voltage range for 3.3V IO pins	-0.3	3.6	V
I/O Voltage range for ADC pins	-0.1	2.1	V
USB_DEV_VBUS (USB OTG2.0)	-0.3	5.5	V

Table 17: Absolute Maximum Ratings

6.2 DC Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
VIN	efus™MX8X input supply voltage	4.5	5	5.5	V
I_{IN}	Input Current			1.0	A
VBAT	RTC Power Supply	2.2	3.0	3.45	V
P_{VBAT}	Power Consumption @85°C		0.22	0.6	µA
USB_DEV_VBUS	USB supply voltage	4.4	5.0	5.5	V
I_{VBUS}	USB supply current		100		mA
V_{ih}	High Level Input Voltage	0.7*OVDD	OVDD		V
V_{il}	Low Level Input Voltage	0	0.3*OVDD		V
I_o	Output current IOs		5.0		mA

Table 18: DC Electrical Characteristics

7 Thermal Specification

The described Embedded Module is a high performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors like housing, power consumption, heat spreader, airflow and many others.

In order to keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
  To reduce heat, the CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS), as well as “Thermal throttling” by an integrated temperature sensor. The integrated sensor measures the temperature of the CPU die and lowers CPU clock or shut down CPU if needed.
  DVFS lowers CPU clock and voltage in accordance with the performance needed from the application.
  For optimal use of DVFS, modify your software to only use peak performance for short times.
- The housing has big influence on the heat dissipation. There are many points to analyze:
  - Is there the option of dissipating heat to the housing?
  - Is there a possibility that the air can circulates in the housing?
  - Is an active cooling possible?
- The surrounding temperatures has a big effect to the temperature of the system.
- Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction.

The following table shows nominal thermal specification of the module:

	Min	Typ.	Max	Unit
Consumer Range Environmental Temperature	0		+70	°C
Consumer Range CPU Junction Temperature	-40		+105	°C
Industrial Range Environmental Temperature (I)	-20		+85	°C
Industrial Range CPU Junction Temperature (I)	-40		+125	°C
Extended Industrial Range Environmental Temperature (XI)	-40		+85	°C
Extended Industrial Range CPU Junction Temperature (XI)	-40		+125	°C
Junction to Package Top (ΨJT)		0.1		°C/W

Table 19: Thermal Specifications

Note 1: Maximum junction temperature of the CPU is 105°C/125°C. In this case cooling is a necessity and highly recommended. See also: *Power Consumption and Cooling*

Note 2: WLAN Module can support only -30°C to +85°C. This component is not critical for the booting operation.

Note 3: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN13273 (https://www.nxp.com/docs/en/application-note/AN13273.pdf)

8 Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

9 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

10 Second Source Rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

11 Power Consumption and Cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **17.0 Watt**. This values are with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **t.b.d. Watt to t.b.d. Watt** on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

12 Storage Conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage, we recommend vacuum dry packs.

13 ROHS and REACH Statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

14 Packaging

All F&S ESD-sensitive products will shipping either in trays or in bags.
These modules ship in trays. One tray can hold 10 boards. An empty tray will be used as top cover.

15 Matrix Code Sticker

All F&S hardware will ship with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 3: Matrix Code Sticker

16 Appendix

Important Notice

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