Hardware Documentation

PicoCore™BBULP for HW Revision 1.30

Preliminary

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About This Document

This document describes how to use the PicoCore™BBULP start interface board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

ESD Requirements



All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	٧	Platform	A,M,R	Chapter	Description	Au
12.09.2019	000	All		-	Initial Version	MD

V Version

A, M, R Added, Modified, Removed

Au Author

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1 Main Features

The following table shows the maximum possible number of each interface. Not all interfaces are available at the same time and depends on the appropriate assembly variant.

Features	Description
Main Board	PicoCore™MX7ULP
DC-Input	+5V ±10% / 5V USB / 4.2V Battery ±10%
Audio	Audio IN/OUT, HP, MIC
Display	2-lane MIPI-DSI
Touch Control	4-wire resistive touch input / capacitive touch via I2C
GPIO	max. 27
Interfaces	1 x USB OTG (Host/Device) 4 x UART (2 x with line flow control, 2 x without line flow control) 4 x I2C 1 x SPI

Table 1: Main Features



2 Mechanical Dimensions

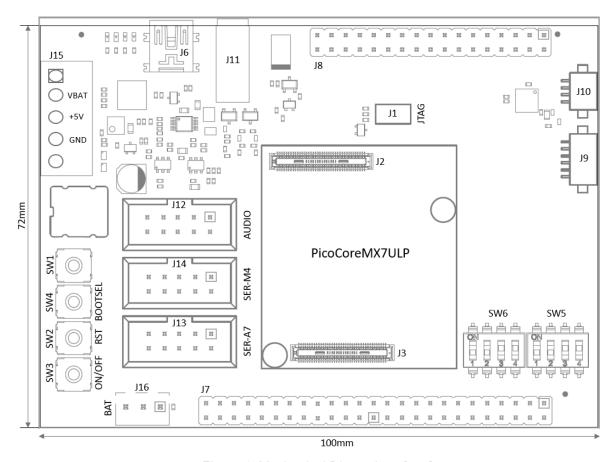


Figure 1: Mechanical Dimensions [mm]

Dimensions	Description
Size	100mm x 72mm
PCB Thickness	1.5mm ± 0.1mm
Height of the parts on the top side	9mm
Height of the parts on the bottom side	2.7mm
Weight	47gr (without PicoCore™MX7ULP Module) 54gr (with PicoCore™MX7ULP Module)

Table 2: Mechanical Dimensions



2.1 Connectors & Switches Layout

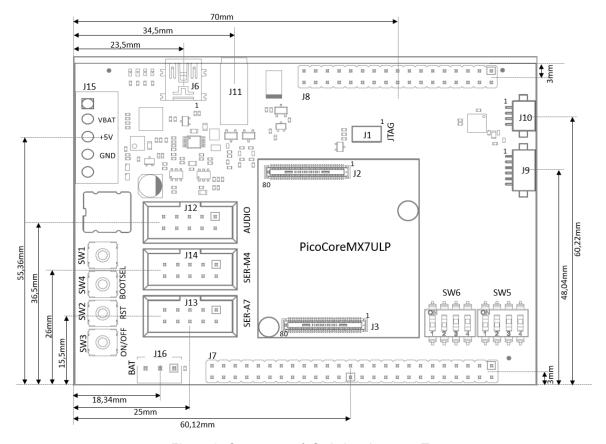


Figure 2: Connectors & Switches Layout - Top

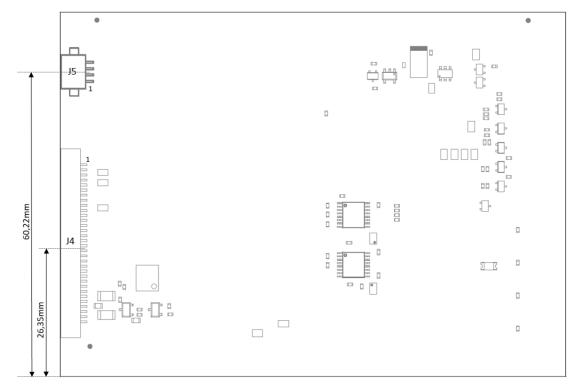


Figure 3: Connectors & Switches Layout - Bottom



Des.	Description	Remarks
J1	JTAG Connector	Top Side, 10-pins
J2	PicoCore Board to Board Connector	Top Side, 80-pins
J3	PicoCore Board to Board Connector	Top Side, 80-pins
J4	Display Connector	Bottom Side, 30-pins
J5	Display Control Connector	Bottom Side, 4-pins
J6	USB Connector	Top Side, Host & Device
J7	GPIO (Feature) Connector	Top Side, 50-pins
J8	GPIO (Feature) Connector	Top Side, 34-pins
J9	I2C Connector	Top Side, 5-pins
J10	Touch Screen Connector	Top Side, 4-pins
J11	Headphone and MIC	Top Side, 3,5mm Jack compatible
J12	Audio IN / OUT	Top Side, 10-pins
J13	UART A7 (Debug Port), RS232 only RXD and TXD	Top Side, 10-pins
J14	UART M4, RS232 with RXD, TXD, RTS and CTS	Top Side, 10-pins
J15	Power Connector	Top Side, 5-pins
J16	Battery Connector	Top Side, 3-pins
SW1	Tamper Detection Button	Top Side, Tact Switch
SW2	Reset In Button	Top Side, Tact Switch
SW3	On/Off Button	Top Side, Tact Switch
SW4	Boot Select Button	Top Side, Tact Switch
SW5	SPI/I2C Selection Switch	Top Side, Coding Switch
SW6	SPI/I2C Selection Switch	Top Side, Coding Switch

Table 3: Connectors & Switches List



3 Interface and signal description

3.1 B2B connectors (J2 and J3)

Type: DF40C-80DS-0.4V (51) [or another pin compatible connector with different height]

Manufacturer: Hirose

Please refer the PicoCore module datasheet for pin-out assignments.

3.2 Power Supply

The PicoCore base board has a 5 way connector with 3,81mm pitch for an external DC power supply.

Connector Base Board: Würth WR-TBL Series 322 – 5- pins

Matching Connector: Würth WR-TBL Series 2109

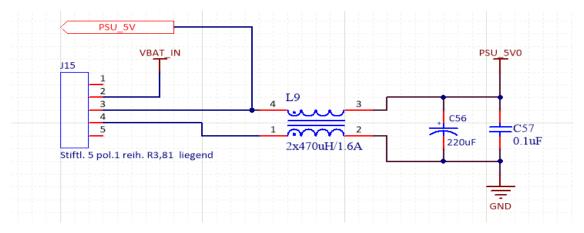


Figure 4: Power Supply Connector

J15 Pin	Signal Name	I/O	Remarks
1	NC		
2	VBAT_IN	PWR	Voltage: 2.2V-3.45V (*Optional for external RTC voltage supply)
3	PSU_5V0	PWR	Voltage: 4.5V-5.5V
4	GND	PWR	
5	NC		

Table 4: Power Connector Pin Layout



4 Interfaces

4.1 USB OTG

The USB OTG port can operate as device or as a host port. The USB differential signals are routed with an impedance of 90Ω .

Connector type: Würth USB2.0 mini-B

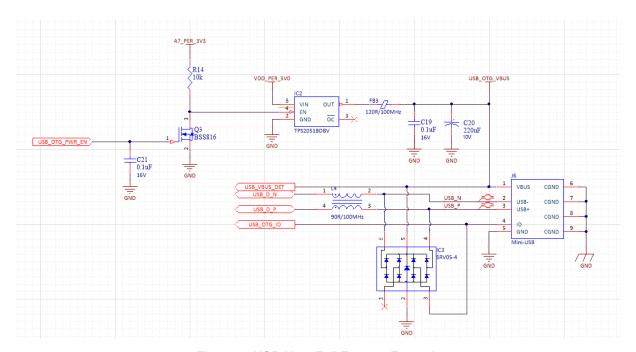


Figure 5: USB Host Full Feature Example

J6 Pin	Signal Name	PicoCore Pin Number	I/O	Voltage	Remarks
1	USB_OTG_VBUS		PWR	5V	Input in device mode and output in host mode
2	USB_OTG_N	J3-75	I/O diff		Differential data line routed with 90Ω
3	USB_OTG_P	J3-77	I/O diff		Differential data line routed with 90Ω
4	USB_OTG_ID	J3-78	I	1.82V	
5	GND		PWR	GND	

Table 5: USB OTG Interface Pin Layout



4.2 Audio

The PicoCore base board provides a 3.5mm audio jack for the headphone and mic.

Connector type: CUI SJ2-357X-SMT

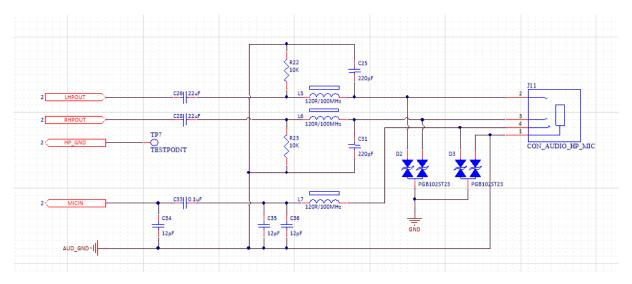


Figure 6: Headphone and Mic

J11 Pin	Signal Name	PicoCore Pin Number	I/O	Voltage	Remarks
1	AUDIO_GND	J2-79	PWR	GND	
2	LHPOUT	J2-75	0		
3	RHPOUT	J2-77	0		
4	MICIN	J2-80	I		

Table 6: Headphone Jack Pin Layout



On the PicoCore Baseboard there is also a connector (J12) for the Audio IN and OUT signals. Connector type: FCI 75869

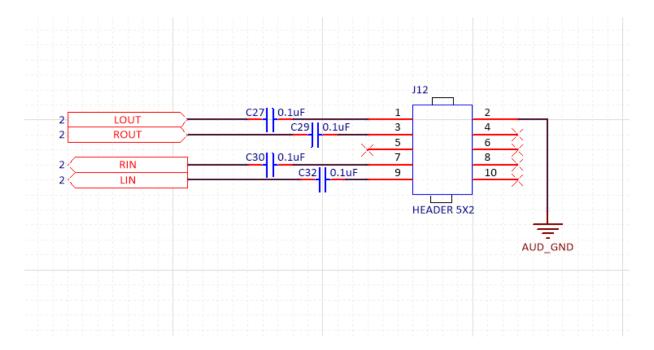


Figure 7: Audio Connector

J12 Pin	Signal Name	PicoCore Pin Number	I/O	Voltage	Remarks
1	LOUT	J2-68	0		
2	AUD_GND	J2-66/72/78	PWR	GND	
3	ROUT	J2-70	0		
4	NC	Х	Х	Х	
5	NC	Х	Х	Х	
6	NC	Х	Х	Х	
7	RIN	J2-76	I		
8	NC	Х	X	Х	
9	LIN	J2-74	I		
10	NC	Х	Х	Х	

Table 7: Audio Connector Pin Layout



4.3 MIPI-DSI Display

The PicoCore base board provides a 30-pin connector for the MIPI-DSI display.

Connector type: ES&S STE-FI-X30S-HF-NPB-TW

J4 Pin	Signal Name	PicoCore Pin Number	I/O	Voltage	Remarks
1	DSI_DATA0_N	J2-26	I/O		
2	DSI_DATA0_P	J2-24	I/O		
3	DSI_DATA1_N	J2-38	I/O		
4	DSI_DATA1_P	J2-36	I/O		
5	NC	X	Χ	X	
6	NC	X	X	X	
7	GND		PWR	GND	
8	DSI_CLK_N	J2-32	I/O		
9	DSI_CLK_P	J2-30	1/0		
10	NC	X	Χ	X	
11	NC	X	X	X	
12	NC	X	Χ	Х	
13	NC	X	Χ	X	
14	GND		PWR	GND	
15	NC	X	Χ	X	
16	NC	X	Χ	X	
17	GND		PWR	GND	
18	NC	X	Χ	Х	
19	NC	X	Χ	X	
20	NC	X	Χ	Х	
21	NC	X	Χ	X	
22	NC	X	X	X	
23	NC	X	Х	X	
24	GND		PWR	GND	
25	TOUCH_SDA	J2-58	1/0	3.3V	Shared with J9
26	TOUCH_IRQ#	J2-25	I	3.3V	Shared with J9
27	TOUCH_SCL	J2-60	1/0	3.3V	Shared with J9
28	MIPI_RESET#	J2-27	I	3.3V	
29	VLCD		PWR	3.3V	
30	VLCD		PWR	3.3V	

Table 8: MIPI Display Connector Pin Layout



To control the LCD voltage and backlight, backlight control connector (J5) have to be used properly. Bypassing this connector and using the LCD with "Backlight Always On" mode, the FB1 has to be assembled. (FB1: 700R/90MHz-1206-Ferrite Bead)

J5 Pin	Signal Name	PicoCore Pin Number	I/O	Voltage	Remarks
1	VLCD_ON	J3-38	1/0	3.3V	Display on/off
2	BL_ON	J3-36	I/O	3.3V	Backlight on/off
3	BL_PWM	J2-29	1/0		Backlight Brightness
4	GND		PWR	GND	

Table 9: I²C Touch Control Interface

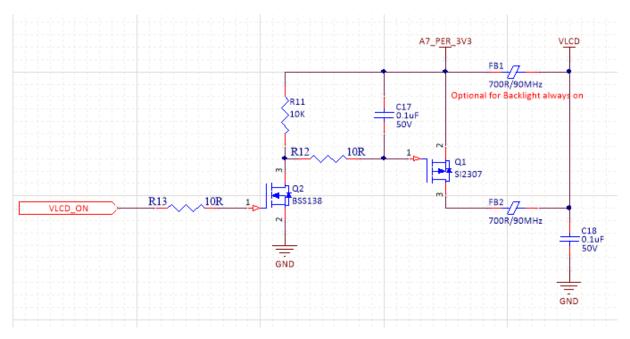


Figure 8: LCD Voltage Control



4.4 Touch Control Interface

PicoCore supports both 4/5-wire resistive touch control and capacitive proximity sensing via I²C with Semtech SX8675 (IC4). The baseboard provides a 6-pin connector (J9) for the I²C signals and a 4-pin connector (J10) for the electrode signals in order to use touch control interface.

Connector types: Hirose DF13-6P-1.25H (20) - J9

Hirose DF13-4P-1.25H (20) - J10

J9 Pin	Signal Name	PicoCore Pin Number	I/O	Voltage	Remarks
1	A7_PER_3V3		PWR	3.3V	
2	TOUCH_SDA	J2-58	1/0	3.3V	Shared with J4
3	TOUCH_SCL	J2-60	1/0	3.3V	Shared with J4
4	TOUCH_RST#	J2-20	0	3.3V	
5	TOUCH_IRQ#	J2-25	ı	3.3V	Shared with J4
6	GND		PWR	GND	

Table 10: I²C Touch Control Interface

J10 Pin	Signal Name	PicoCore Pin Number	I/O	Voltage	Remarks
1	A7_PER_3V3		PWR	3.3V	
2	TOUCH_SDA	J2-58	I/O	3.3V	Shared with J4
3	TOUCH_SCL	J2-60	I/O	3.3V	Shared with J4
4	TOUCH_RST#	J2-20	0	3.3V	
5	TOUCH_IRQ#	J2-25	I	3.3V	Shared with J4
6	GND		PWR	GND	

Table 11: Touch Control Interface Data Signals



4.5 Feature Connectors

The PicoCore base board provides two feature connectors with 50 pins (J7) and 34 pins (J8).

J7 Pin	Signal Name	PicoCore Pin Number	I/O	Voltage	Remarks
1	A7_PER_3V3		PWR	3.3V	
2	VDD_PER_3V3		PWR	3.3V	
3	PTC16	J3-40	1/0	1.8V	GPIO
4	PTC17	J3-42	1/0	1.8V	GPIO
5	PTC18	J3-44	I/O	1.8V	GPIO
6	PTF3	J3-64	I/O	3.3V	GPIO
7	PTF6	J3-58	I/O	3.3V	GPIO
8	PTF7	J3-56	I/O	3.3V	GPIO
9	PTF8	J3-54	I/O	3.3V	GPIO
10	PTF9	J3-52	I/O	3.3V	GPIO
11	GND		PWR	GND	
12	SPI3_SCK	J3-63	I	3.3V	
13	UART7_TX	J2-54	0	3.3V	
14	SPI3_CS0	J3-61	I	3.3V	
15	UART7_RX	J2-56	I	3.3V	
16	A7_PER_3V3 / SPI3_SIN / I2C5_SCL	- / J3-67 / J3- 62	1/0	3.3V	Depends on the position of the code switch.
17	A7_PER_3V3 / SPI3_SOUT / I2C5_SDA	- / J3-65 / J3- 60	1/0	3.3V	Depends on the position of the code switch.
18	PTF11	J3-48	I/O	3.3V	GPIO
19	PTF10	J3-50	I/O	3.3V	GPIO
20	DAC1_OUT	J2-71	0		
21	DACO_OUT	J2-69	I		
22	PTC9	J3-28	I/O	1.8V	GPIO
23	NC	X	X	Х	
24	PTC12	J3-32	I/O	1.8V	GPIO
25	PTC11	J3-30	1/0	1.8V	GPIO
26	PTC13	J3-34	I/O	1.8V	GPIO
27	GND		PWR	GND	
28	NC	Х	Х	Х	
29	UART6_CTS	J2-31	0	VDD_PTE	
30	NC	Х	Х	Х	
31	UART6_RTS	J2-33	I	VDD_PTE	
32	A7_PER_1V8		PWR	1.8V	



J7 Pin	Signal Name	PicoCore Pin Number	I/O	Voltage	Remarks
33	UART6_TX	J2-35	I	VDD_PTE	
34	M4_PER_3V3		PWR	3.3V	
35	UART6_RX	J2-37	0	VDD_PTE	
36	UART5_RX	J2-47	0	V1.8V	
37	GND		PWR	GND	
38	UART5_TX	J2-45	I	1.8V	
39	A7_PER_3V3		PWR	3.3V	
40	VDD_PER_5V0		PWR	5.0V	
41	MICIN	J2-80	I		
42	GND		PWR	GND	
43	NC	X	Χ	Χ	
44	RIN	J2-76	I		
45	ROUT	J2-73	0		
46	GND		PWR	GND	
47	GND		PWR	GND	
48	LIN	J2-74	I		
49	LOUT	J2-68	0		
50	GND		PWR	GND	

Table 12: 50-pin Feature Connector Pin Layout



J8 Pin	Signal Name	PicoCore Pin Number	I/O	Voltage	Remarks
1	A7_PER_1V8		PWR	1.8V	
2	A7_PER_3V3		PWR	3.3V	
3	VDD_PTE		PWR	VDD_PTE	
4	M4_PER_3V3		PWR	3.3V	
5	PTA3	J3-41	1/0	3.3V	GPIO
6	VDD_PER_5V0		PWR	5.0V	
7	PTA13	J3-37	I/O	3.3V	GPIO
8	PTA12	J3-39	I/O	3.3V	GPIO
9	SEN_INT#	J2-52	ı		
10	I2C0_SDA	J2-65	I/O	3.3V	
11	I2CO_SCL	J2-63	I/O	3.3V	
12	PTB2	J3-49	I/O	1.8V	GPIO
13	PTB3	J3-51	I/O	1.8V	GPIO
14	PTB10	J3-53	I/O	1.8V	GPIO
15	PTB11	J3-55	I/O	1.8V	GPIO
16	GND		PWR	GND	
17	PTB14	J3-57	I/O	1.8V	GPIO
18	PTA14	J3-35	I/O	3.3V	GPIO
19	PTA15	J3-33	I/O	3.3V	GPIO
20	PTA23	J3-31	I/O	3.3V	GPIO
21	PTA31	J3-29	I/O	3.3V	GPIO
22	PTB1	J3-47	I/O	1.8V	GPIO
23	UART2_CTS	J2-48	ı	3.3V	
24	I2C3_SDA	J2-51	I/O	1.8V	
25	UART2_RTS	J2-46	0	3.3V	
26	I2C3_SCL	J2-49	I/O	1.8V	
27	UART2_TX	J2-42	0	3.3V	
28	GND		PWR	GND	
29	UART2_RX	J2-44	I	3.3V	
30	GND		PWR	GND	
31	GND		PWR	GND	
32	GND		PWR	GND	
33	GND		PWR	GND	
34	GND		PWR	GND	

Table 13: 34-pin Feature Connector Pin Layout



4.6 **Buttons and Switches**

On PicoCore™BBULP baseboard there are 4 buttons to operate general preset functions.

Ref.	Signal Name	PicoCore Pin Number	Function	Usage
SW1	TAMPER_DET	J3-17	Tamper Detection	X
SW2	RESETIN#	J3-10	Reset CPU	Normal Push to Reset CPU
SW3	IMX_ON/OFF	J3-7	CPU On/Off	1 Second-Long Push to ON 5-Seconds-Long Push to OFF
SW4	BOOTSEL#	J2-64	Boot Selection	X

Table 14: Buttons and their Functions

There are also 2 coding switches on the baseboard in order to choose optional SPI3 and I2C5 serial interfaces.

Ref.	Pin Number	Usage
SW5	J7-16	 Pull-Up for the Chosen Data Line (Use when necessary) SPI3_SIN I2C5_SCL NC
SW6	J7-17	 Pull-Up for the Chosen Data Line (Use when necessary) SPI3_SOUT I2C5_SDA NC

Table 15: Coding Switches Pin Layout



4.7 Serial Interface Connectors (J13 & J14)

J13 connector is for debugging A7 Core with 1.8V logic level. (UART4: without line flow control)

J14 connector is for debugging M4 Core with 3.3V logic level. (UART0: with line flow control lines RTS and CTS)

J13 Pin	Signal Name	PicoCore Pin Number	I/O	Voltage	Remarks
1	NC	Х	Х	Х	
2	NC	X	Х	Х	
3	RX4				→ UART4_RX
4	NC	Х	Х	Х	
5	TX4				→ UART4_TX
6	NC	X	X	X	
7	NC	X	X	X	
8	NC	X	X	X	
9	GND		PWR	GND	
10	VCC_COM		PWR	5V	

Table 16: J13 Pin Layout

J14 Pin	Signal Name	PicoCore Pin Number	I/O	Voltage	Remarks
1	NC	X	Х	X	
2	NC	X	Х	Х	
3	RX0				→ UART4_RX
4	RTS0	X	Х	Х	→ PTA1
5	TX9				→ UART4_TX
6	CTS0	X	Χ	X	→ PTAO
7	NC	X	Χ	X	
8	NC	X	Χ	X	
9	GND		PWR	GND	
10	VCC_COM		PWR	5V	

Table 17: J14 Pin Layout



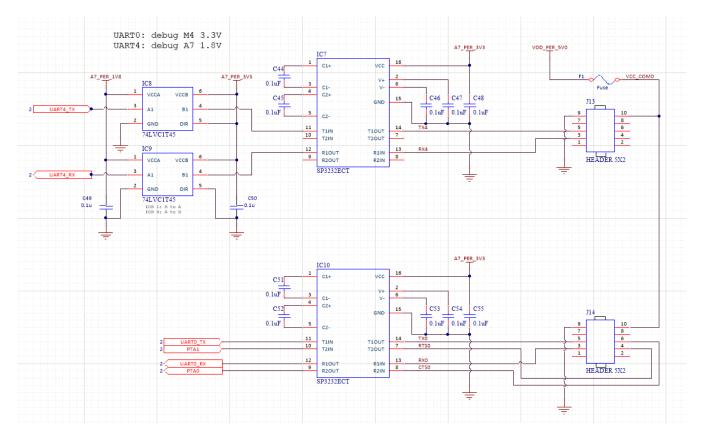


Figure 9: Serial Debug Interface Schematic



Electrical Characteristic 5

5.1 **Power Inputs**

Signal Name	Connector	Remarks
PSU_5V0	J15 – Pin3	OVDD*+0.3
VBAT_IN¹	J15 – Pin2	RTC battery input voltage
USB_OTG_VBUS ²	J6 – Pin1	USB input supply voltage
VBAT_4V2	J16 – Pin1	Battery input supply voltage
GND	GND, connect all GND pins to GND	a plane

^{1:} Leave open if not used 2: Input in device mode

Table 18: Power Inputs

5.2 **Recommended Operation Conditions**

Parameter	Description	Min.	Тур.	Max.	Unit
PSU_5V0	Power Supply Voltage	4.5	5.0	5.5	V
VBAT_IN	RTC Supply Voltage	2.2	3.0	3.45	V
VBAT_4V2	Battery Supply Voltage	3.78	4.2	4.62	V
USB_OTG_VBUS	USB Supply Voltage	4.5	5.0	5.5	V

Table 19: Recommended Operation Conditions



6 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

7 ESD and EMI Implementation

On the PicoCoreBBULP base board there are ESD protection diodes for Mini-USB and Audio Jack connectors. The other connectors do not have any protection, because of their immunity to ESD. To reduce EMI the PicoCoreMX7ULP supports Spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

A helpful guide is available from TI; just search for slva680 at ti.com.

8 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

9 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.

Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here. Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.



10 Matrix Code Sticker

All F&S hardware will ship with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.



Figure 10: Matrix Code Sticker



11 Appendix

Important Notice

The information in this publication has been carefully checked and is believed to be entirely accurate at the time of publication. F&S Elektronik Systeme ("F&S") assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained in this documentation.

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