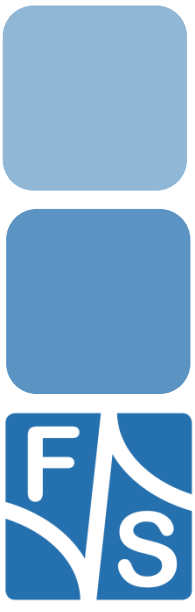
LCD Module Specification

FS-T070QYH-13CP R001

Preliminary

Version 001

(2022-05-25)



Elektronik Systeme

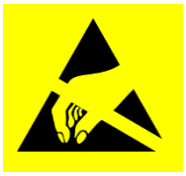
© F&S Elektronik Systeme GmbH
Untere Waldplätze 23
D-70569 Stuttgart
Fon: +49(0)711-123722-0
Fax: +49(0)711 – 123722-99

About This Document

This document describes how to use the FS-T070QYH-13C LCD module with mechanical and electrical information. The latest version of this document can be found at:

https://www.fsembedded.com

ESD Requirements



All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
2022-05-17	001		-	-	Initial release	UK

V	Version
A,M,R	Added, Modified, Removed
Au	Author

Table of Contents

1 General Description

The FS-T070QYH-13CP combines an 7” MIPI-DSI Display, a capacitive touch panel (CTP), bonded to a cover glass, and an interface board.

Item	Content	Unit
LCD Type	TFT	-
Display color [1]	16.7 M	colors
Viewing Direction	ALL	O’Clock
Active Area (W x H)	94.2 x 150.7	mm
Number of Dots	800 x 1280	dots
Driver ICs	GT928 (LCD), FT5426 (CTP)	-
Backlight	8S5P-LEDs (white)	-
Interface	MIPI	-
Modul size (W x H x D)	123.2 x 191.9 x 10.4	mm
Weight	200	g
Operating Temperature	0 … +50	°C
Storage Temperature	-10 … +60	°C

Table 1: General Description

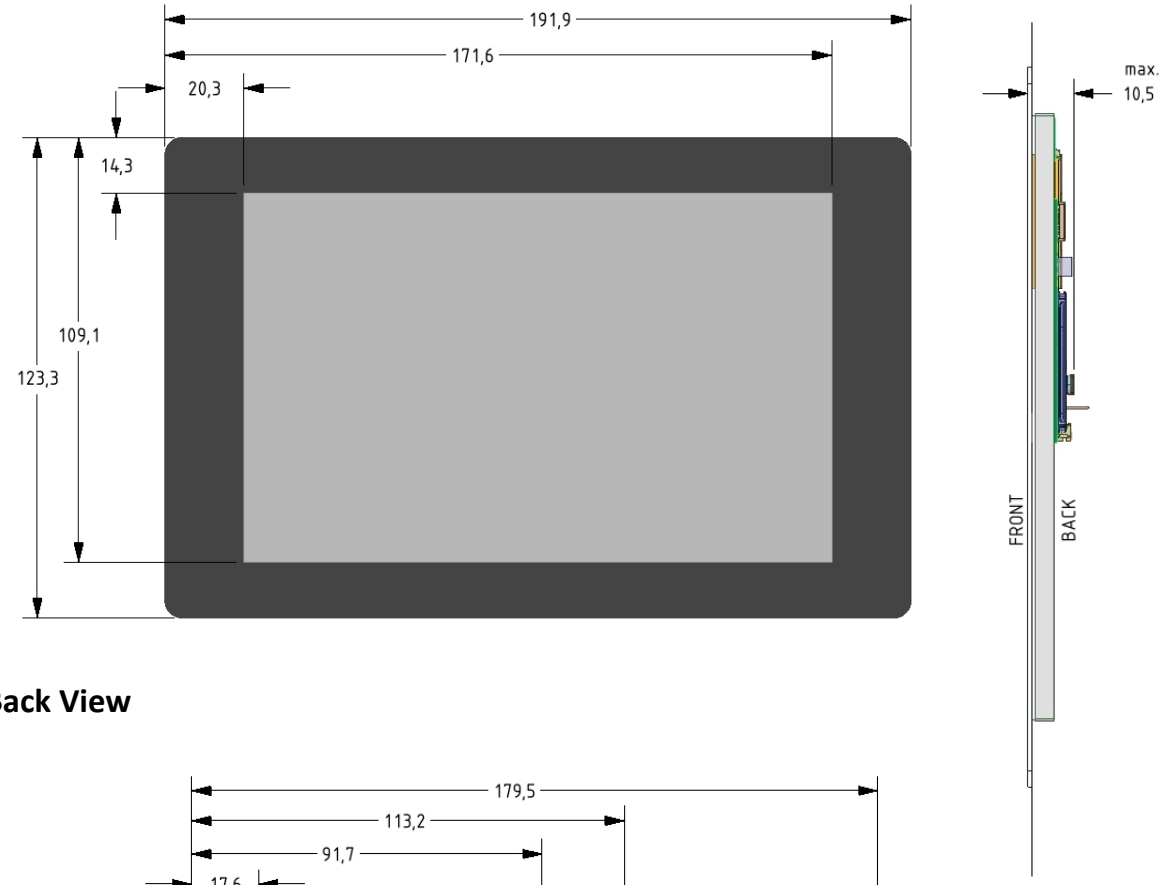
Note 1: *Color tune is slightly changed by temperature and driving voltage.*

Figure 1: FS-T070QYH-13CP

2 Mechanical Characteristics

Front View

Side View



Back View

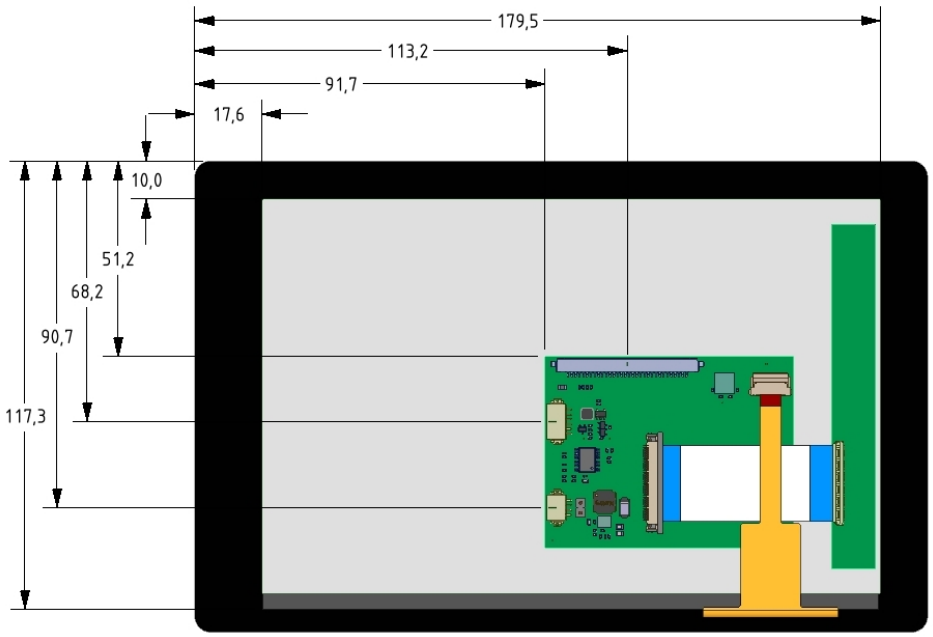


Figure 2: Mechanical Characteristics

Note: *All Dimensions are in mm.*

3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
LCD supply voltage [1, 2]	V_{LCD}	-0.3	5.5	V
CTP supply voltage [1, 2]	V_{I2C}	2.7	3.6	V
Backlight supply voltage [1, 2]	V_{BL_IN}	4	10	V
Operating Temperature [3, 4]	T_{OP}	0	+50	°C
Storage Temperature	T_{ST}	-10	+60	°C
Humidity [5] ($T_{AMB} \leq 40$ °C)	-	-	85	% RH

Table 2: Absolute Maximum Ratings

Note 1: T_{AMB} = 25 °C

Note 2: *If the voltages exceed these absolute maximum ratings, the module may become permanently damaged.*

Note 3: *The response time will become lower at low temperature.*

Note 4: *Background color changes slightly, depending on T_{AMB}.*

Note 5: T_{AMB} > 40 °C: *Absolute humidity must be lower than 85 % RH.*

4 Electrical Characteristics

4.1 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
LCD supply voltage [1]	V_{LCD}	3.0	3.3	3.6	V
CTP supply voltage [1]	V_{I2C}	2.8	-	3.3	V
Backlight supply voltage [1]	V_{BL_IN}	4.5	5.0	5.5	V

Table 3: Recommended Operation Conditions

Note 1: T_{AMB} = 25 °C

4.2 Backlight Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Power Consumption	P_{BL}	2.5	2.8	3.1	W
Uniformity (I_f = 100 mA)	ΔBp	75	80	-	%
Life Time [1] (I_f = 100 mA)		20000	-	-	hours

Table 4: Backlight Characteristics

Note 1: *Brightness to be reduced to 50 % of the initial value at T_{AMB} = 25 °C.*

4.3 Interface Description

4.3.1 Connector List and Types

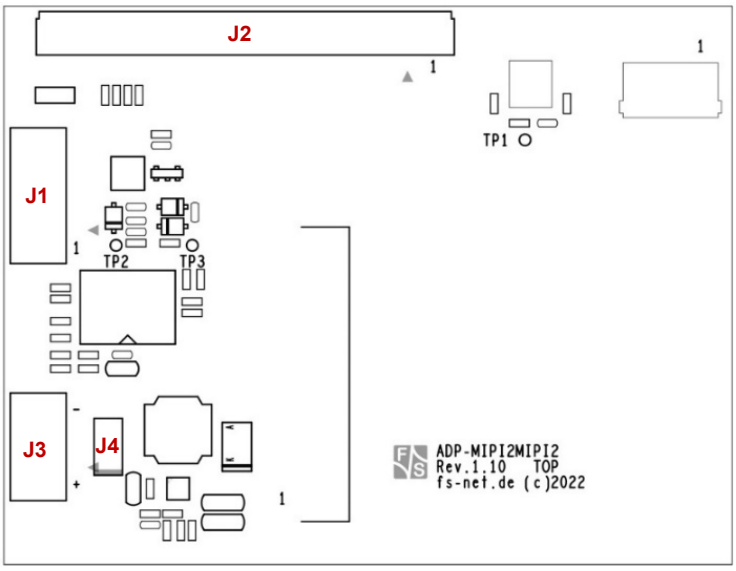


Figure 3: Connector Positions

Ref.	Description	No. of Pins	Connector Type	Mating Connector
J1	Touch Controller Input	6	DF13-6P-1.25H	DF13-6S-1.25C
J2	MIPI-DSI Input	30	FI-X30SSLA-HF	FI-X30H & FI-X30HL
J3	Backlight Supply	4	DF13-4P-1.25H	DF13-4S-1.25C
J4	Backlight Supply	2	Pin Header (2.54 mm)	-

Table 5: Connector List and Types

4.3.2 Connector Pin Description

J1 is the baseboard-side-connection of the Touch Controller (TC) / Backlight control [1] / LCD Reset [1].

Pin	Signal Name	I/O	Voltage	Description
1	VI2C	PWR	3.3 V	TC supply voltage
2	I2C2_SDA	I/O	3.3 V	I2C Serial Data
3	I2C2_SCL	I	3.3 V	I2C Clock
4	I2C2_RST	I	3.3 V	I2C Reset
5	I2C2_IRQ	O	3.3 V	I2C Interrupt Request
6	GND			

Table 6: J1 Pin Description

Note 1: *via PCA9634PW, I2C-address: 0x61*

J2 is the baseboard-side-connection of the LCD.

Pin	Signal Name	I/O	Voltage	Description
1	DSI_A_DATA0_N	I		DSI Chanel A Data Lane 0-
2	DSI_A_DATA0_P	I		DSI Chanel A Data Lane 0+
3	DSI_A_DATA1_N	I		DSI Chanel A Data Lane 1-
4	DSI_A_DATA1_P	I		DSI Chanel A Data Lane 1+
5	DSI_A_DATA2_N	I		DSI Chanel A Data Lane 2-
6	DSI_A_DATA2_P	I		DSI Chanel A Data Lane 2+
7	GND			
8	DSI_A_CLK_N	I		DSI Chanel A Clock Signal-
9	DSI_A_CLK_P	I		DSI Chanel A Clock Signal+
10	DSI_A_DATA3_N	I		DSI Chanel A Data Lane 3-
11	DSI_A_DATA3_P	I		DSI Chanel A Data Lane 3+
12	N.C.	X		not connected
13	N.C.	X		not connected
14	GND			
15	N.C.	X		not connected
16	N.C.	X		not connected
17	GND			
18	N.C.	X		not connected
19	N.C.	X		not connected
20	N.C.	X		not connected
21	N.C.	X		not connected
22	N.C.	X		not connected
23	N.C.	X		not connected
24	GND			
25	I2C2_SDA	I/O	3.3 V	I2C Serial Data (not used)
26	I2C2_IRQ	O	3.3 V	I2C Interrupt Request (not used)
27	I2C2_SCL	I	3.3 V	I2C Clock (not used)
28	I2C2_RST	I	3.3 V	I2C Reset (not used)
29	VLCD	PWR	3.3 V	LCD supply voltage
30	VLCD	PWR	3.3 V	LCD supply voltage

Table 7: J2 Pin Description

J3 is the baseboard-side-connection for the Backlight (BL) supply voltage.

Pin	Signal Name	I/O	Voltage	Description
1	VBL_IN	PWR	5 V	BL supply voltage
2	VBL_IN	PWR	5 V	BL supply voltage
3	GND			
4	GND			

Table 8: J3 Pin Description

J4 is an alternative connection for the Backlight supply voltage.

Pin	Signal Name	I/O	Voltage	Description
1	VBL_IN	PWR	5 V	BL supply voltage
2	GND			

Table 9: J4 Pin Description

4.4 AC Electrical Characteristics

4.4.1 High speed Mode

Signal	Symbol	Parameter	Min	Typ	Max	Unit	Description
DSI-CLK+/-	2xUIINST	Double UI instantaneous	4	-	8	ns	4 Lane [2]
			3	-	8	ns	3 Lane [2]
			2.352	-	8	ns	2 Lane [3]
DSI-CLK+/-	UIINSTA UIINSTB	UI instantaneous halfs (UI = UIINSTA = UIINSTB)	2	-	4	ns	4 Lane [2]
			1.5	-	4	ns	3 Lane [2]
			1.176	-	4	ns	2 Lane [3]
DSI-Dn+/-	tDS	Data to clock setup time	0.15x UI	-	-	ps	
DSI-Dn+/-	tDH	Data to clock hold time	0.15x UI	-	-	ps	
DSI-CLK+/-	tDRTCLK	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDRTDATA	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	tDFTCLK	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDFTDATA	Differential fall time for data	150	-	0.3xUI	ps	

Table 10: High Speed Mode

Note 1: *Dn = D0, D1, D2 and D3.*

Note 2: *Maximum total bit rate is 2 Gbps for 24-bit data format, 1.5 Gbps for 18-bit data format and 1.33 Gbps for 16-bit data format in 3 lanes or 4 lanes application which support up to 800 x 1280 resolution.*

Note 3: *Maximum total bit rate is 1.7 Gbps for 24-bit data format, 1.275 Gbps for 18-bit data format and 1.13 Gbps for 16-bit data format in 2 lanes application which support up to 720 x 1280 resolution.*

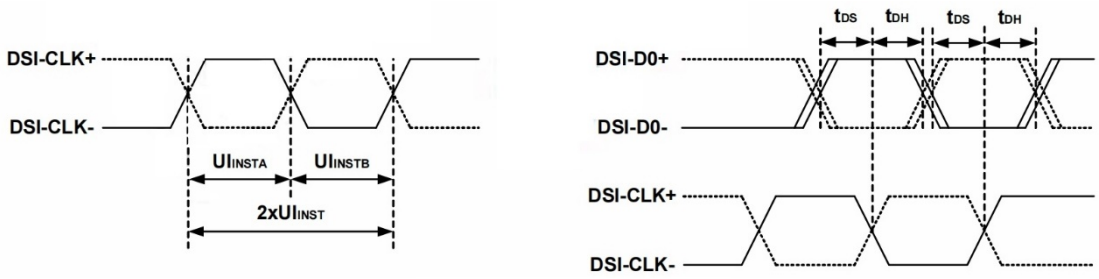


Figure 4: DSI Clock Channel Timing

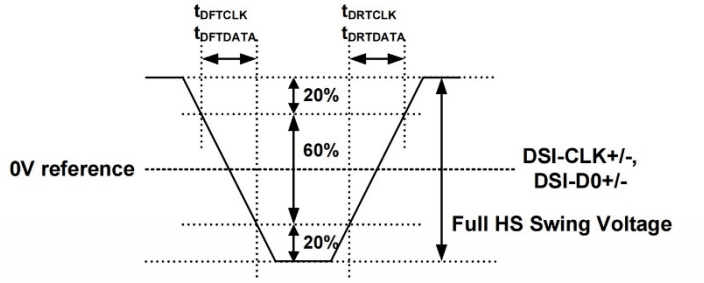


Figure 5: Rise and Fall Time on Clock and Data Channel

4.4.2 LP Transmission

Parameter	Symbol	Min	Typ	Max	Unit
DSI CLK frequency (LP)	F_{DSICLK_LP}			10	MHz
DSI CLKCycle Time (LP)	t_{CLKC_LP}	100			ns
DSI Data Transfer Rate (LP)	t_{DSIR_LP}			10	Mbps
15% - 85% rise/fall time	T_{RLP}/T_{FLP}	-	-	35	ns
30% - 85% rise time (from HS to LP)	T_{REOT}	-	-	35	ns
Pulse width of the LP exclusive-OR clock	$t_{LP\text{-}PULSE\text{-}TX}$	50	65	-	ns
Period of the LP exclusive-OR clock	$t_{LP\text{-}PRE\text{-}TX}$	100	130	-	ns

Table 11: LP Transmission

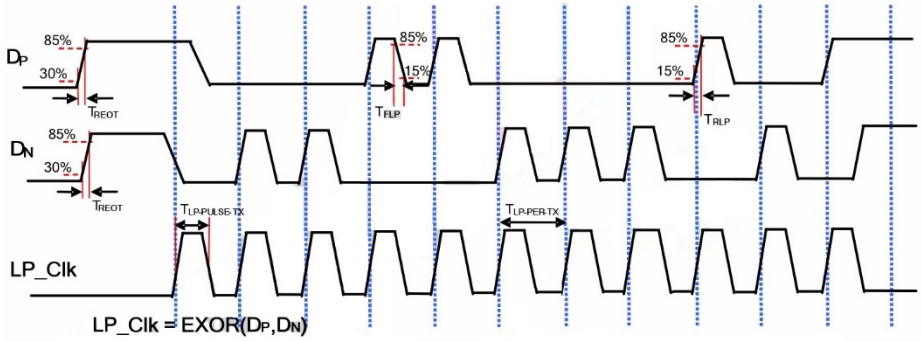


Figure 6: LP Transmission

4.4.3 Low Power Mode

Signal	Symbol	Parameter	Min	Typ	Max	Unit	Desription
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods (Display Module)	50	-	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods (Display Module)	50	-	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2xTLPXD	ns	Output
DSI-D0+/-	TTA-DETD	Time to drive LP-00 by display module	5xTLPXD	-		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request - MPU	4xTLPXD	-		ns	Output

Table 12: LP Transmission

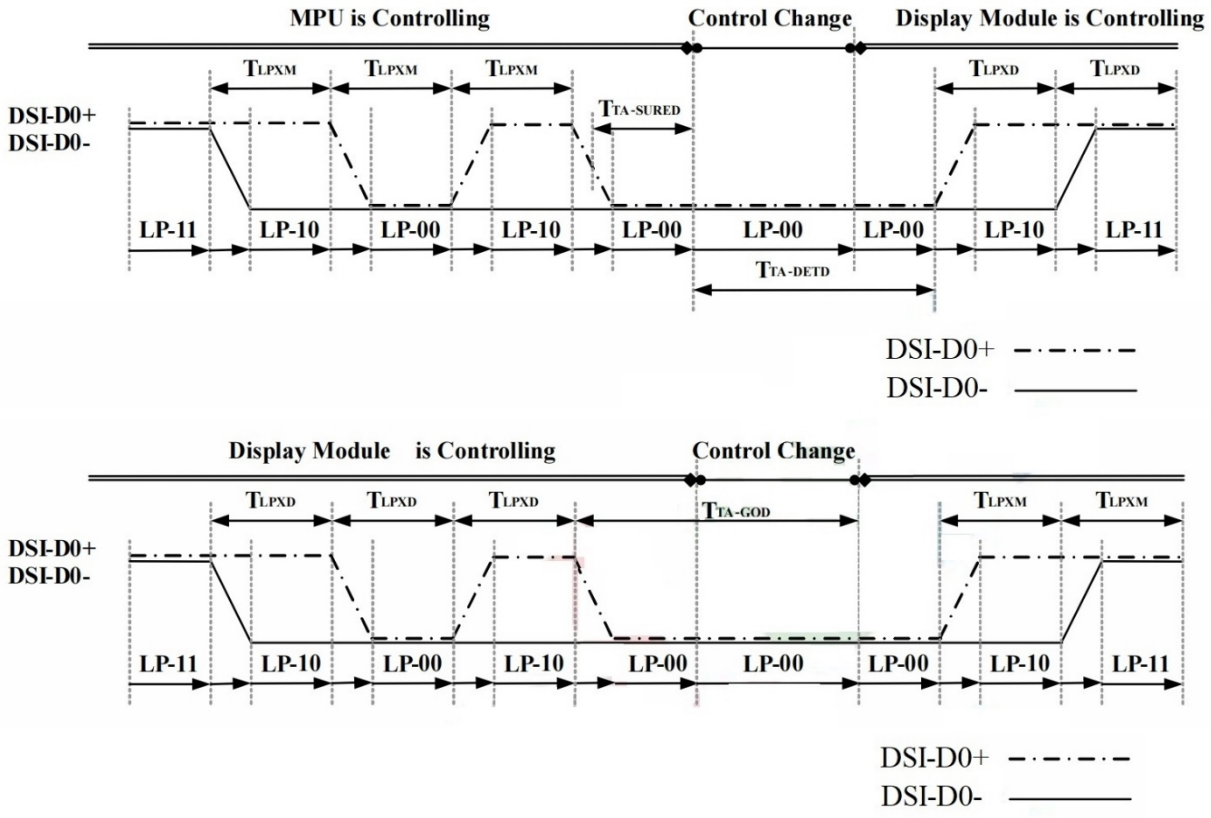


Figure 7: Bus Turnaround (BAT) from MPU to Display Module Timing

4.4.4 DSI Bursts

Signal	Symbol	Parameter	Min	Typ	Max	Unit	Desription
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE +TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Table 13: DSI Bursts

Note 1: *Dn = D0, D1, D2 and D3.*

Note 2: *Two HS transmission can be sent with a break as short as THS-EXIT from each other in continuous clock mode. In discontinuous mode, the break is longer which account TCLK-POS, TCLK-TRAIL and THS-EXIT, before the activity in clock and data lanes.*

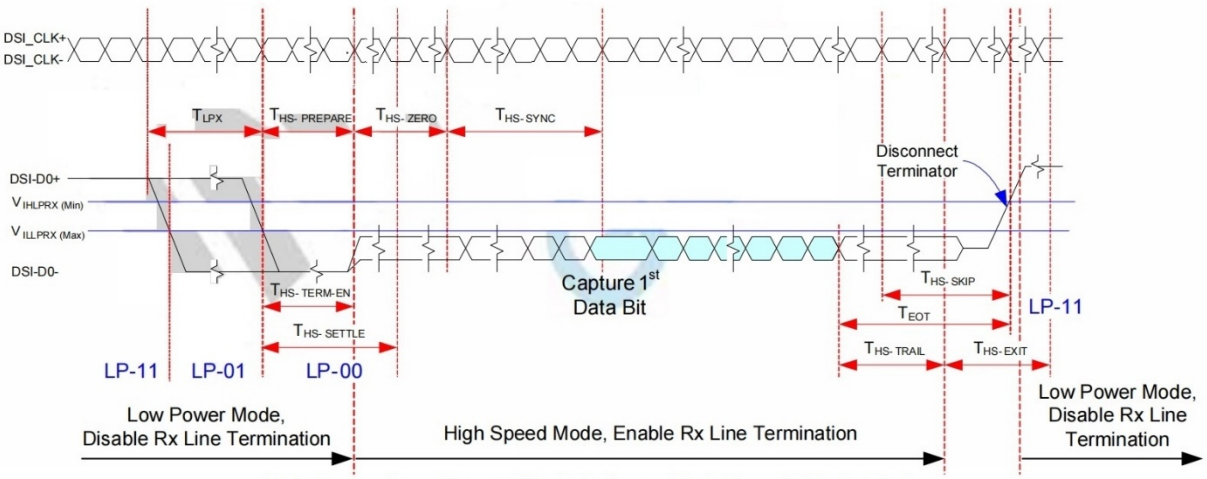


Figure 8: Data Lanes - Low Power Mode to/from High Speed Mode Timing

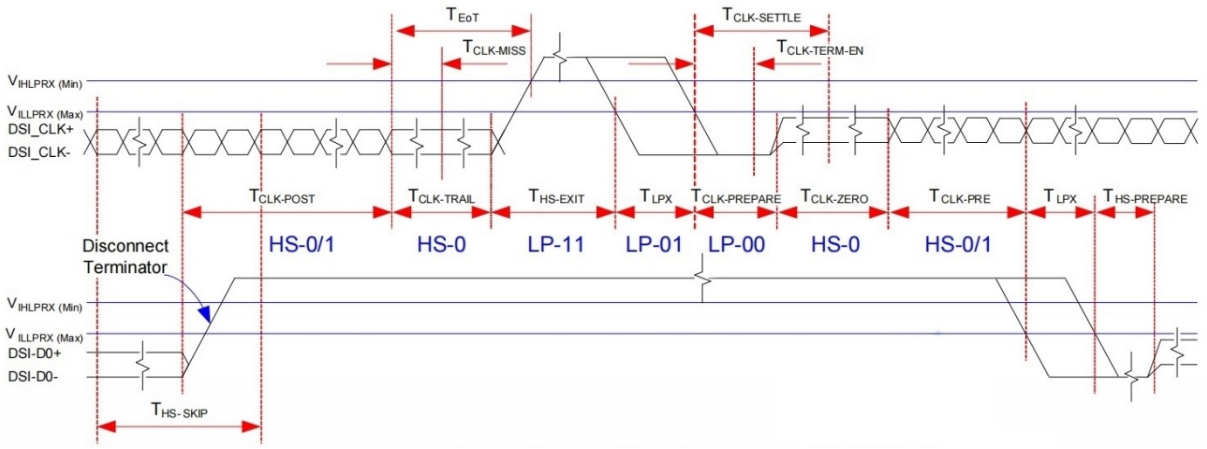


Figure 9: Clock Lanes - High Speed Mode to/from Low Power Mode Timing

4.4.5 Reset Input Timing

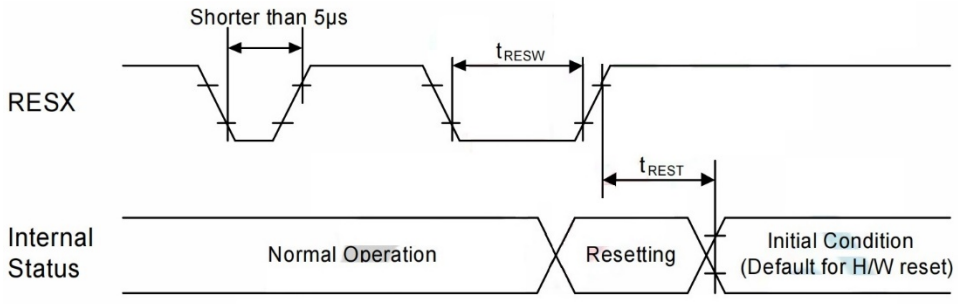


Figure 10: Reset Input Timing

Signal	Symbol	Parameter	Min	Typ	Max	Unit	Desription
RESX	t_{RESW}	Reset "L" pulse width [1]	10	-	-	µs	
	t_{REST}	Reset complete time [2]	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and [5]

Table 14: Reset Input Timing

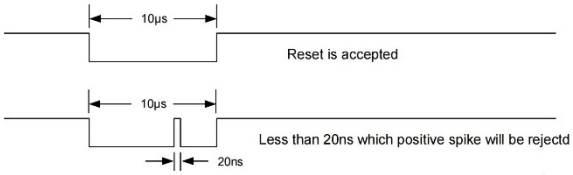
Note 1: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the taple below.

RESX Pulse	Action
Shorter than 5 µs	Reset rejected
Longer than 10 µs	Reset
Between 5 µ and 10 µs	Reset Start

Note 2: *During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when reset starts in Sleep Out-mode. The display remains the blank state in Sleep In-mode.) and them return to Default condition for H/W reset.*

Note 3: *During reset complete time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5 ms after rising edge of RESX.*

Note 4: *Spike rejection also applies during a valid reset pulse as shown below:*



Note 5: *It is necessary to wait 5 ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 ms.*

4.4.6 Deep Standby Mode Timing

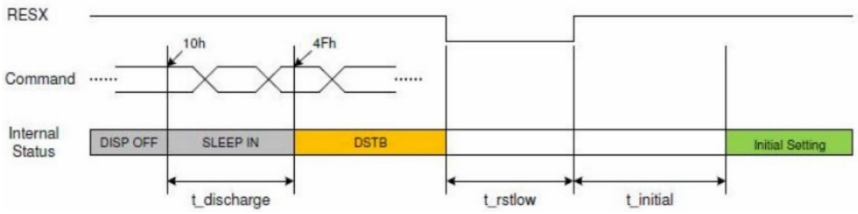


Figure 11: Deep Standby Mode Timing

Signal	Symbol	Parameter	Min	Typ	Max	Unit	Desription
RESX	$t_{discharge}$	Sleep in into DSTB delay time	-	-	100	ms	
	t_{rstlow}	Rest low pulse	3	-	-	ms	
	$t_{initial}$	Reset high to initial setting delay time	-	-	120	ms	

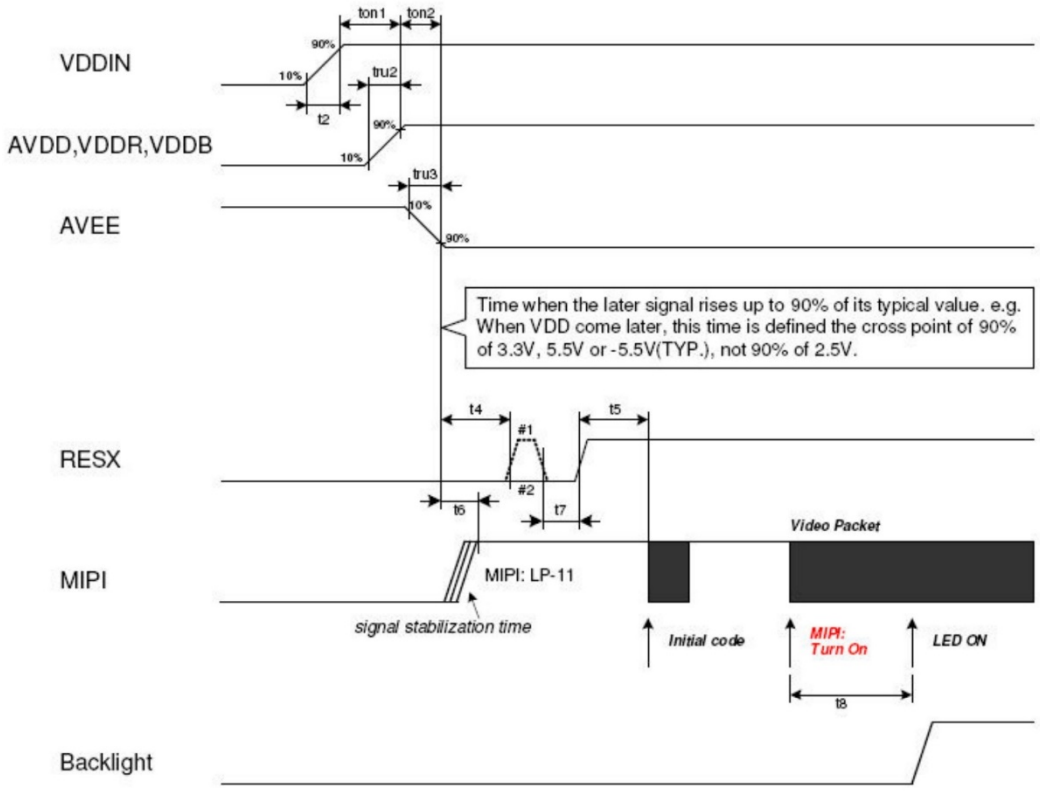
Table 15: Deep Standby Mode Timing

Note 1: *$t_{discharge}$ suggested delay time. more than 100 ms*

Note 2: *$t_{initial}$ suggested delay time. more than 120 ms*

4.5 Power Sequence

4.5.1 Power on



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note 2: This power-on sequence is based on adding schottky diode on VGLX pin to ground.

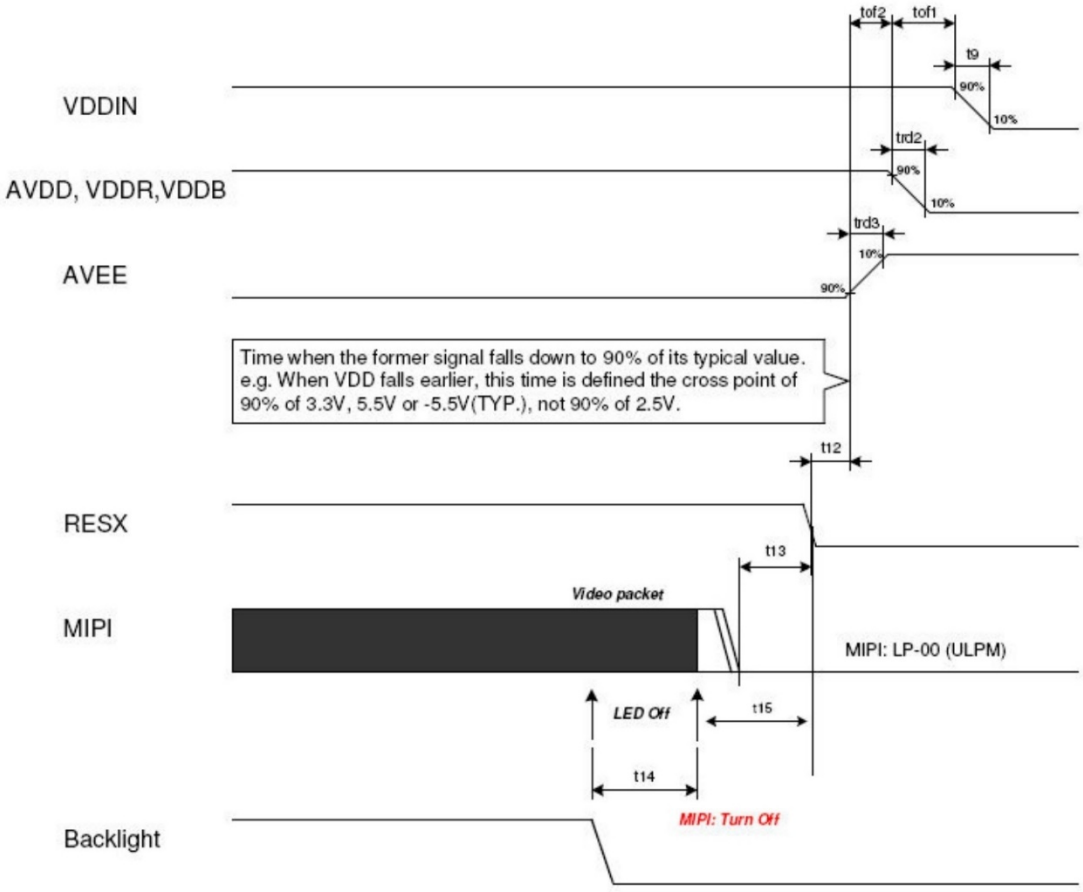
Note 3: Reset signal H to L to H (#1) is better than only L to H (#2).

Figure 12: Power On Sequence

Symbol	Min	Typ	Max	Unit	Remark
ton1	-	No limit	-	ms	
ton2	-	0 (Note)	-	ms	
t2	-	-	150	ms	
tru2	-	-	150	ms	
tru3	-	-	150	ms	
t4	40	-	-	ms	
t5	120	-	-	ms	
t6	0	-	-	ms	
t7	10	-	-	µs	
t8	8	-	-	VS	Keep data more than 8 frames (VS)

Table 16: Power On Timing

4.5.2 Power off



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Figure 13: Power Off Sequence

Symbol	Min	Typ	Max	Unit	Remark
t9	150	-	-	µs	
tof1	-	No limit	-	ms	
tof2	-	0 (Note)	150	ms	
trd2	150	-	150	µs	
trd3	150	-	150	µs	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	0	-	-	ms	
t15	10	-	-	ms	

Table 17: Power Off Timing

5 Optical Characteristics

Item	Symbol		Condition	Min	Typ	Max	Unit
Brightness [1]	Bp		θ = 0° Φ = 0°	-	700	-	Cd / m²
Uniformity [1, 2]	⊿Bp			75	80	-	%
Viewing Angle [3]	3:00		Cr ≥ 10	-	80	-	Deg
	6:00			-	80	-	
	9:00			-	80	-	
	12:00			-	80	-	
Contrast Ratio [4]	Cr		θ = 0° Φ = 0°	600	800	-	-
Response Time [5]	T_r+T_f			-	20	25	ms
Color of CIE Coordinate [1, 6]	W	x	θ = 0° Φ = 0°	0.26	-	0.32	-
		y		0.27	-	0.33	-
	R	x		Typ. -0.05	-	Typ. +0.05	-
		y			-		-
	G	x			-		-
		y			-		-
	B	x			-		-
		y			-		-
NTSC Ratio	S			45	60	-	%

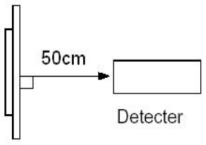
Table 18: Optical Characteristics

Note: *The parameter is slightly changed by temperature, driving voltage and materiel.*

Note 1: *The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment BM-7 (Φ5 mm)*

Measuring condition:
- *Measuring surroundings: Dark room.*
- *Measuring temperature: Ta=25℃.*
- *Adjust operating voltage to get optimum contrast at the center of the display.*

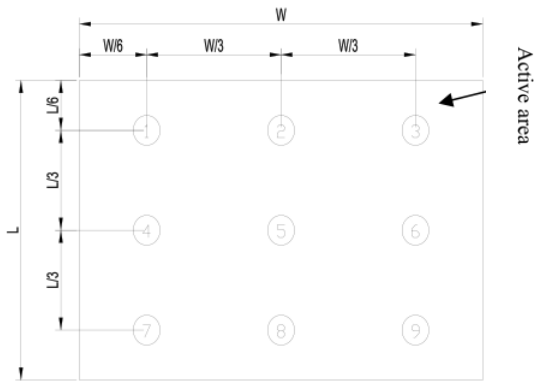
Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.



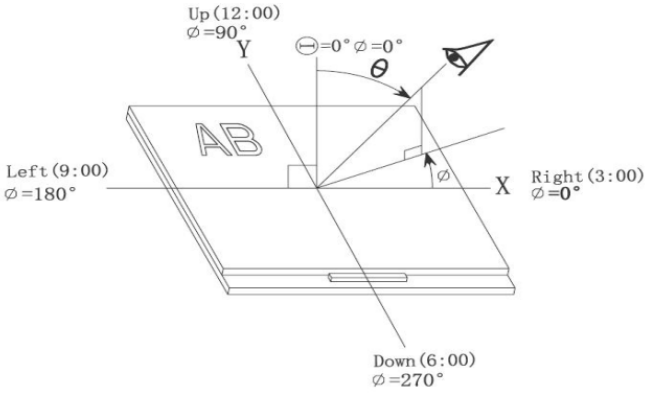
Note 2: *The luminance uniformity is calculated by using following formula.*

⊿Bp = Bp (Min.) / Bp (Max.) × 100 (%)

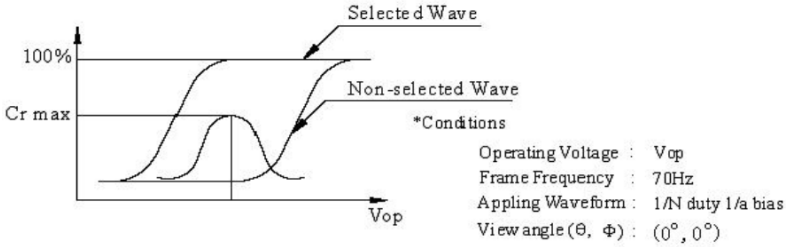
Bp (Max.) = Maximum brightness in 9 measured spots
Bp (Min.) = Minimum brightness in 9 measured spots.



Note 3: *The definition of viewing angle: Refer to the graph below marked by θ and Φ*



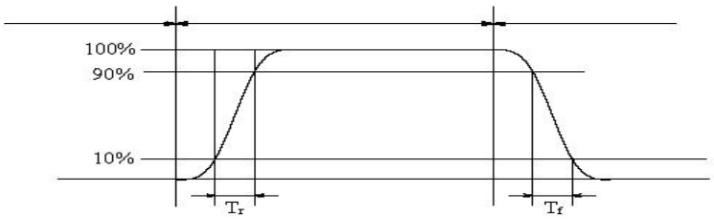
Note 4: *Definition of contrast ratio.(Test LCD using DMS501)*



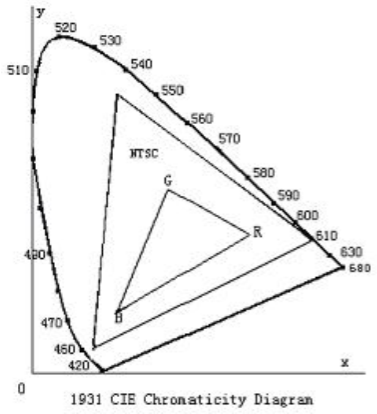
$$Contrast\ ratio(Cr) = \frac{Brightness\ of\ selected\ dots}{Brightness\ of\ non-selected\ dots}$$

Note 5: *Definition of Response time. (Test LCD using DMS501):*

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (falling time) and from "white" to "black" (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 6: *Definition of Color of CIE Coordinate and NTSC Ratio.*



Color gamut:

$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

6 Reliability Test Items and Criteria

Test Item	Test Condition
High Temperature Storage [1, 3, 4]	T_a = +60 °C (96 hrs)
Low Temperature Storage [1, 3, 4]	T_a = -10 °C (96 hrs)
High Temperature Operation [2, 3, 4]	T_s = +50 °C (96 hrs)
Low Temperature Operation [2, 3, 4]	T_s = 0 °C (96 hrs)
Operation at High Temperature / Humidity [3, 4]	+40 °C, 90% RH (96 hrs)
Thermal Shock [3, 4]	-10 °C (30 min) … +60 °C (30 min), 10 cycles Start with cold temperature and end with high temperature
Vibration Test	Frequency range: 10 … 55 Hz Stroke: 1.5 mm Sweep: 10 Hz … 55 Hz … 10 Hz 2 hours for each direction of x, y, z (6 hours total)
Mechanical Shock	100 G, 6ms, ±x, ±y, ±z 3 times for each direction
Package Vibration Test	Random vibration: 0.015 G * G/Hz, 5 … 200 Hz -6 dB/Octave, 200 … 500 Hz 2 hours for each direction of x, y, z (6 hours total)
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces
Electro Static Discharge	± 2 kV, Human Body Mode, 100 pF / 1500 Ω

Table 19: Reliability Test Items and Criteria

Note 1: *T_a is the ambient temperature of samples*

Note 2: *T_s is the temperature of panel's surface*

Note 3: *In the start condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.*

Note 4: *Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.*

7 Precautions for the Use of LCD Modules

7.1 Handling Precautions

1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

   - Isopropyl alcohol
   - Ethyl alcohol

   Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

   - Water
   - Ketone
   - Aromatic solvents

6. Do not attempt to disassemble the LCD Module.

7. If the logic circuit power is off, do not apply the input signals.

8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

   a. Be sure to ground the body when handling the LCD Modules.

   b. Tools required for assembly, such as soldering irons, must be properly ground.

   c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

   d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

7.2 Storage Precautions

1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

2. The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature:	0 °C … 40 °C
Relatively humidity	≤ 80 %

3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

7.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

8 Second Source Rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.
F&S does not use broker components without the consent of the customer.

9 Storage Conditions

Maximum storage on room temperature with non-condensing humidity:	6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity:	12 months

For longer storage we recommend vacuum dry packs.

10 ROHS and REACH Statement

All F&S designs are created from lead-free components and are completely ROHS compliant. The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

11 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 14: Matrix Code Sticker

12 Appendix

Important Notice

The information in this publication has been carefully checked and is believed to be entirely accurate at the time of publication. F&S Elektronik Systeme assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained in this documentation.
F&S Elektronik Systeme reserves the right to make changes in its products or product specifications or product documentation with the intent to improve function or design at any time and without notice and is not required to update this documentation to reflect such changes.
F&S Elektronik Systeme makes no warranty or guarantee regarding the suitability of its products for any particular purpose, nor does F&S Elektronik Systeme assume any liability arising out of the documentation or use of any product and specifically disclaims any and all liability, including without limitation any consequential or incidental damages.
Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.
Products are not designed, intended, or authorized for use as components in systems intended for applications intended to support or sustain life, or for any other application in which the failure of the product from F&S Elektronik Systeme could create a situation where personal injury or death may occur. Should the Buyer purchase or use a F&S Elektronik Systeme product for any such unintended or unauthorized application, the Buyer shall indemnify and hold F&S Elektronik Systeme and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that F&S Elektronik Systeme was negligent regarding the design or manufacture of said product.
Specifications are subject to change without notice.

Warranty Terms

Hardware Warranties
F&S guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and F&S's sole liability shall be for F&S, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

Software Warranties
Software is provided "AS IS". F&S makes no warranties, either express or implied, with regard to the software object code or software source code either or with respect to any third party materials or intellectual property obtained from third parties. F&S makes no warranty that the software is useable or fit for any particular purpose. This warranty replaces all other warranties written or unwritten. F&S expressly disclaims any such warranties. In no case shall F&S be liable for any consequential damages.

Disclaimer of Warranty

THIS WARRANTY IS MADE IN PLACE OF ANY OTHER WARRANTY, WHETHER EXPRESSED, OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A SPECIFIC PURPOSE, NON-INFRINGEMENT OR THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION, EXCEPT THE WARRANTY EXPRESSLY STATED HEREIN. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDIES OF ANY PURCHASER WITH RESPECT TO ANY DEFECTIVE PRODUCT.

Limitation on Liability

UNDER NO CIRCUMSTANCES SHALL F&S BE LIABLE FOR ANY LOSS, DAMAGE OR EXPENSE SUFFERED OR INCURRED WITH RESPECT TO ANY DEFECTIVE PRODUCT. IN NO EVENT SHALL F&S BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES THAT YOU MAY SUFFER DIRECTLY OR INDIRECTLY FROM USE OF ANY PRODUCT. BY ORDERING THE PRODUCT, THE CUSTOMER APPROVES THAT THE F&S PRODUCT, HARDWARE AND SOFTWARE, WAS THOROUGHLY TESTED AND HAS MET THE CUSTOMER'S REQUIREMETS AND SPECIFICATIONS

13 Content