Application Note OSM01

OSM Implementation Guide

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Elektronik Systeme

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About This Document

When integrating an *Open Standard Module*™ (OSM), defined by *the Standardization Group for Embedded Technology e. V.* (SGeT), several special topics are to be considered. The intention of this document is to give all necessary information for the implementation. The document focuses on the general requirements of the F&S Modules. The latest version of this document can be found at: www.fs-net.de.

ESD Requirements

All F&S hardware products are electrostatic discharge (ESD) sensitive. All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD sensitive material in ESD unsafe environments. Negligent handling will harm the product and warranty claims become void.

Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

History

Version/Date	Platform	Added (A) Removed (R) Modified (M)	Chapter	Description	Author
001/08.2024	All	A	All	Initial Version	UK
002/11.2024	-	M	All	Drawing of the shipping tray added, minor adaptions	UK
003/04.2025	-	M	3.1	Drawing of the shipping tray corrected	UK
004/04.2025	-	A, M, R	All	New design template, major adaptions	UK
005/08.2025	-	A	2.1.2, 3.3	Processing information added	MC, UK
006/04.2026	-	M	2.2.2, 2.2.7, 2.2.9	Note regarding voltage options added	UK
007/09.2026	-	M	2.2.15	Information regarding PUs on USB_B & USB_C added	UK

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1 Overview

1.1 Additional Documentation

F&S highly recommends reading the following documents besides the implementation process:

- OSM HW Specification V1.2 (as of 08/11/2024, available at https://sget.org, login required)
- OSM Design Guide 1.0 (as of 04/05/2022, available at https://sget.org, login required)[1]

[1] Contains a step-by-step implementation description with circuit examples.

1.2 Design Data

F&S provides a set of OSM design data (Altium & Cadence), including

- schematic symbols (general & module-specific implementation information),
- footprints (including position references & footprints for the spacers of the F&S heat spreader),
- 3D models of the modules,

to ease the implementation. The design data (including schematics) of a suitable carrier board are also available and may be used as reference. The latest versions of the design data can be downloaded from www.fs-net.de.

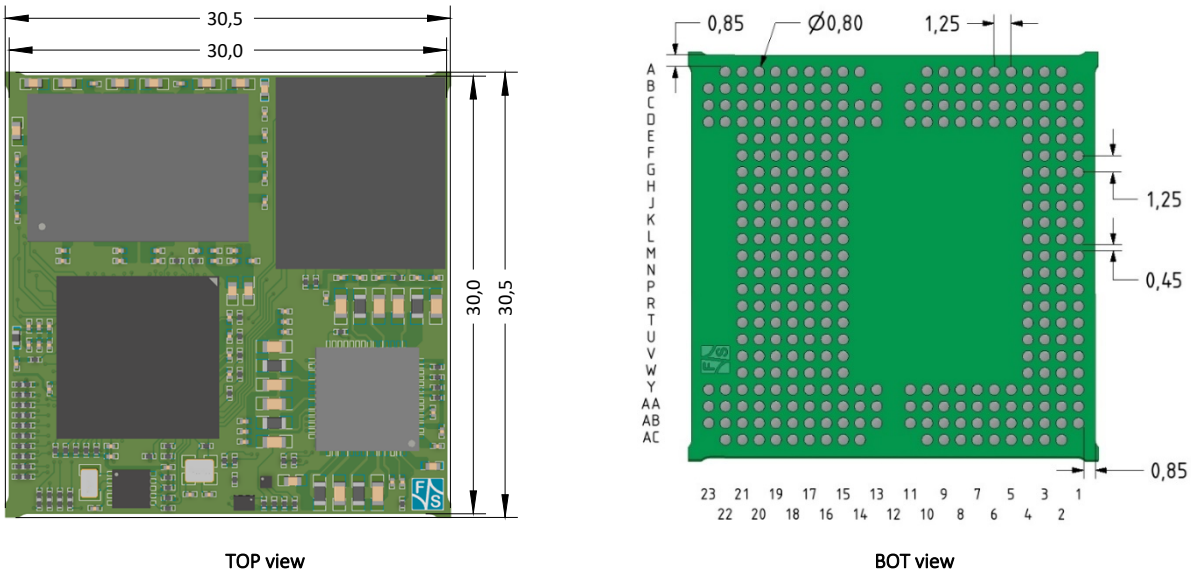
2 Design Process

2.1 Mechanical Information

2.1.1 Dimensions

All F&S modules are assembled on one side. Neither a PCB-spacer nor a cut-out on the carrier board is required. All modules are Standard Height F - “Flat” modules according to the specification.

Due to the production process, all F&S modules have a small overhang at the corners which must be considered.



TOP view

BOT view

Note: All dimensions are in mm.

Figure 1: OSM Size-S (dimensions)

2.1.2 Contact Characteristics

By default, the contact type is an Electroless Nickel Immersion Gold Land Grid Array (ENIG LGA). Fused Tin Grid Array (FTGA) finish is optionally available.

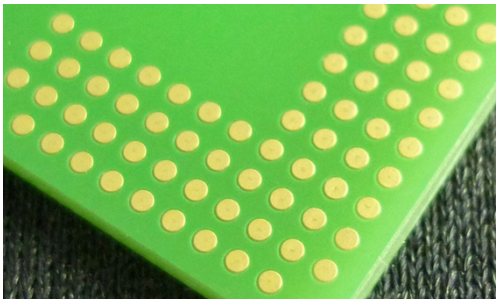


Figure 2: LGA example

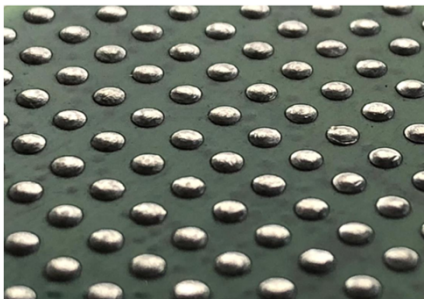


Figure 3: FTGA example

When to choose which?

LGA, when you need the lowest z-height[1], want maximum storage robustness, and have SPI and stencil experience to control paste volume at a cost-efficient module price.

FTGA, when you want more process tolerance to warpage / coplanarity and wetting, outgassing under the part matters, and you can manage pre-tin oxidation and adjust paste volume to avoid bridging.

[1] An internal validation yielded an LGA standoff height of approx. 75 µm when using a 100 µm stencil and SAC305 (Type ≥ 4) in vapor-phase reflow.

Criterion	LGA	FTGA
Pad Finish	ENIG (Electroless Nickel Immersion Gold)	pre-tinned SAC305 (via stencil & reflow)
Shelf Life / Oxidation	long Au surface is oxidation-tolerant	short exposed SnAgCu is oxidation-prone -> prefer dry/N_2 storage and prompt use after opening
MSL / Floor-Life Handling	MSL 3 (same as FTGA)	MSL 3 (same as LGA)
Solder Volume Control	defined entirely by PCB stencil	combined volume (module & PCB)
Bridging risk	low with 1:1 aperture	higher aperture-reduction recommended
Self-Alignment	medium accurate placement important	slightly improved wetting from pre-tin
Handling Robustness	high less sensitive to fingerprints / contamination	medium sensitive to fingerprints / contamination

Table 1: Contact Characteristics

2.1.3 Cooling

As basis for a cooling concept, F&S offers a heat spreader. Part number is MHS.OSM.1, including:

- 1x heat spreader plate
- 1x thermal interface material (TIM)
- 4x M2.5x6mm DIN965

For more information, see document “OSM Cooling Solution”. The latest version can be found at: www.fs-net.de.

2.2 Contact Grid Signal Description

The following tables show the complete general contact grid signal description for OSM size-S modules according to the OSM HW Specification V.1.2 with a focus on F&S modules.

2.2.1 Conventions

Contact Type	Description
I	input to the module
O	output from the module
I/O	bi-directional input / output signal
OD	open drain output
I OD	input to the module, where an OD output on the carrier is expected
n.c.	not connected on any F&S module

Table 2: Contact Types (I/O)

Contact Type	Description
P	power to the module
PO	power source from the module
analog	analog signal between defined voltage
CMOS	Logic input or output
USB	USB compatible differential signal
USB SS	USB SuperSpeed compatible differential signal
MIPI CSI	MIPI CSI differential signal (D-PHY or M-PHY)
MIPI DSI	MIPI DSI differential signal (D-PHY)
PCIe	PCI Express compatible differential signal
LVDS	Low Voltage Differential Signal for connecting an LCD

Table 3: Buffer Types

2.2.2 Power & GND

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
M19	VCC_2_TEST[1]	PO	1.8 V		1.8 V for testing purposes max. current: 50 mA
Y16	VCC_3_TEST	PO			PWR testpoint, n.u. on most F&S modules
Y20	VCC_4_TEST	PO	3.3 V		3.3 V supply for carrier peripherals max. current: 200 mA
Y3	VCC_5_TEST	n.c.			
C5	VCC_6_TEST	n.c.			
Y8, Y9, Y10, Y11, Y17,	VCC_IN_5V	P	5.0 V		main power supply input
Y19	VCC_IN_3V3	n.c.			
AA18, AB18	V_BAT	n.c.			
U18	VCC_OUT_IO	PO	1.8 V		general I/O reference voltage max. current: 100 mA
M17	ETH_IOPWR[2]	PO	1.8 V / 2.5 V / 3.3 V		Ethernet I/O reference voltage max. current: 100 mA
C20	SDIO_A_IOPWR[2]	PO	1.8 V / 3.3 V		SDIO_A I/O reference voltage max. current: 100 mA
T20	SDIO_B_IOPWR[2]	PO	1.8 V / 3.3 V		SDIO_B I/O reference voltage max. current: 100 mA
W17	RTC_PWR	P	3.0 V		RTC supply input
A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, D18, E2, E15, E21, F16, F20, H2, H4, J16, J20, L2, L4, L18, M16, M20, P2, P4, P18, R1, R16, R20, U2, U4, V1, V16, V20, W3, Y2, Y18, AA1, AA4, AA7, AA8, AA10, AA11, AA14, AA17, AA19, AA22, AB3, AB6, AB9, AB15, AB21, AC4, AC7, AC10	GND				

Table 4: OSM size-S (PWR & GND pins)

[1] VCC_1_TEST was only used in OSM specification V1.0 only and is no longer available since specification V1.1.

[2] The implemented voltage option depends on the specific module. Please refer to the corresponding module documentation.

2.2.3 System Control

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
V17	CARRIER_PWR_EN	O CMOS	1.8 V		enables power for peripherals on carrier
Y13	CARRIER_STBY#	O CMOS	1.8 V		LOW: module is in standby power state
U17	RESET_IN#	I OD CMOS	1.8 V	PU 10k	LOW: resets module FLOAT: otherwise
Y14	RESET_OUT#	O CMOS	1.8 V		LOW: CPU resets peripherals on carrier

AA9	PWR_BTN#	I OD CMOS	1.8 V … 5.0 V	PU 10k	LOW: behavior depends on configuration FLOAT: in-active state
U19	BOOT_SEL0#	n.c.			
R18	BOOT_SEL1#	n.c.			
T17	FORCE_RECOVERY#	I OD CMOS	1.8 V	PU 10k	

Table 5: OSM size-S (SYS CRTL pins)

2.2.4 MISC

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
N2, AA2, AA13	RESERVED	n.c.			
B22, C16, D6, D7, P16	Vendor Defined				n.c. on most F&S modules
A15, A16, A17, A18, A19, A20, A21, B15, B16, B17, B18, B19, B20, B21, C15, C17, C19, C21	COM_AREA	n.c.			

Table 6: OSM size-S (MISC pins)

2.2.5 JTAG

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
N17	JTAG_TCK(SWCLK)	I CMOS	1.8 V		test clock
N19	JTAG_TMS(SWDIO)	I CMOS	1.8 V		test mode selection
P17	JTAG_TDI	I CMOS	1.8 V		test data input
P19	JTAG_RTCK	O CMOS	1.8 V		returned test clock
R17	JTAG_TDO(SWO)	O CMOS	1.8 V		test data output
R19	JTAG_nTRST	I CMOS	1.8 V		test reset, active LOW
AC18	DEBUG_EN	I CMOS	1.8 V		enables JTAG function
C18	TEST_GENERIC	I/O CMOS	1.8 V		n.c. on most F&S modules

Table 7: OSM size-S (JTAG pins)

2.2.6 UART

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
A14	UART_A_RX	I CMOS	1.8 V		serial data input port A
B13	UART_A_TX	O CMOS	1.8 V		serial data output port A
C13	UART_A_RTS	O CMOS	1.8 V		“Request to Send” handshake port A
C14	UART_A_CTS	I CMOS	1.8 V		“Clear to Send” handshake port A
D14	UART_B_RX	I CMOS	1.8 V		serial data input port B
D13	UART_B_TX	O CMOS	1.8 V		serial data output port B
D15	UART_B_RTS	O CMOS	1.8 V		“Request to Send” handshake port B
D16	UART_B_CTS	I CMOS	1.8 V		“Clear to Send” handshake port B
A22	UART_C_RX	I CMOS	1.8 V		serial data input port C
B23	UART_C_TX	O CMOS	1.8 V		serial data output port C
C22	UART_D_RX	I CMOS	1.8 V		serial data input port D
C23	UART_D_TX	O CMOS	1.8 V		serial data output port D
D22	UART_CON_RX	I CMOS	1.8 V		serial data input console port
D23	UART_CON_TX	O CMOS	1.8 V		serial data output console port

Table 8: OSM size-S (UART pins)

2.2.7 Ethernet

Contact #	Contact Name	I/O Type	I/O Level [2]	PU / PD	Comments
E16	ETH_A_RGMII_CRS	n.c.			
F15	ETH_A_RGMII_COL	n.c.			
H15	ETH_A_RGMII_TXD0	O CMOS	1.8 V / 2.5 V / 3.3 V		transmit data bit 0 port A
G15	ETH_A_RGMII_TXD1	O CMOS	1.8 V / 2.5 V / 3.3 V		transmit data bit 1 port A
H16	ETH_A_RGMII_TXD2	O CMOS	1.8 V / 2.5 V / 3.3 V		transmit data bit 2 port A
G16	ETH_A_RGMII_TXD3	O CMOS	1.8 V / 2.5 V / 3.3 V		transmit data bit 3 port A
K16	ETH_A_RGMII_TX_EN(_ER)	O CMOS	1.8 V / 2.5 V / 3.3 V		Transmit enable (error) port A
J15	ETH_A_RGMII_TX_CLK	I/O CMOS	1.8 V / 2.5 V / 3.3 V		transmit clock port A
K15	ETH_A_RGMII_RXD0	I CMOS	1.8 V / 2.5 V / 3.3 V		receive data bit 0 port A

Contact #	Contact Name	I/O Type	I/O Level [2]	PU / PD	Comments
L15	ETH_A_RGMII_RXD1	I CMOS	1.8 V / 2.5 V / 3.3 V		receive data bit 1 port A
N15	ETH_A_RGMII_RXD2	I CMOS	1.8 V / 2.5 V / 3.3 V		receive data bit 2 port A
P15	ETH_A_RGMII_RXD3	I CMOS	1.8 V / 2.5 V / 3.3 V		receive data bit 3 port A
L16	ETH_A_RGMII_RX_ER	n.c.			
M15	ETH_A_RGMII_RX_DV(_ER)	I CMOS	1.8 V / 2.5 V / 3.3 V		receive data valid port A
R15	ETH_A_RGMII_RX_CLK	I/O CMOS	1.8 V / 2.5 V / 3.3 V		receive clock port A
N16	ETH_A_SDP	n.c.			
T15	ETH_A_MDIO[1]	I/O CMOS	1.8 V / 2.5 V / 3.3 V		ETH management bus data signal port A
T16	ETH_A_MDC[1]	O CMOS	1.8 V / 2.5 V / 3.3 V		ETH management bus clock signal port A
D2	ETH_B_RGMII_CRS	n.c.			
E1	ETH_B_RGMII_COL	n.c.			
G1	ETH_B_RGMII_TXD0	O CMOS	1.8 V / 2.5 V / 3.3 V		transmit data bit 0 port B
F1	ETH_B_RGMII_TXD1	O CMOS	1.8 V / 2.5 V / 3.3 V		transmit data bit 1 port B
G2	ETH_B_RGMII_TXD2	O CMOS	1.8 V / 2.5 V / 3.3 V		transmit data bit 2 port B
F2	ETH_B_RGMII_TXD3	O CMOS	1.8 V / 2.5 V / 3.3 V		transmit data bit 3 port B
J2	ETH_B_RGMII_TX_EN(_ER)	O CMOS	1.8 V / 2.5 V / 3.3 V		Transmit enable (error) port B
H1	ETH_B_RGMII_TX_CLK	I/O CMOS	1.8 V / 2.5 V / 3.3 V		transmit clock port B
J1	ETH_B_RGMII_RXD0	I CMOS	1.8 V / 2.5 V / 3.3 V		receive data bit 0 port B
K1	ETH_B_RGMII_RXD1	I CMOS	1.8 V / 2.5 V / 3.3 V		receive data bit 1 port B
M1	ETH_B_RGMII_RXD2	I CMOS	1.8 V / 2.5 V / 3.3 V		receive data bit 2 port B
N1	ETH_B_RGMII_RXD3	I CMOS	1.8 V / 2.5 V / 3.3 V		receive data bit 3 port B
K2	ETH_B_RGMII_RX_ER	n.c.			
L1	ETH_B_RGMII_RX_DV(_ER)	I CMOS	1.8 V / 2.5 V / 3.3 V		receive data valid port B
P1	ETH_B_RGMII_RX_CLK	I/O CMOS	1.8 V / 2.5 V / 3.3 V		receive clock port B
M2	ETH_B_SDP	n.c.			
C7	ETH_B_MDIO	I/O CMOS	1.8 V / 2.5 V / 3.3 V		ETH management bus data signal port B
C6	ETH_B_MDC	O CMOS	1.8 V / 2.5 V / 3.3 V		ETH management bus clock signal port B

Table 9: OSM size-S (Ethernet pins)

[1] Also used for ETH_B on some F&S modules.

[2] The implemented voltage option depends on the specific module. Please refer to the corresponding module documentation.

2.2.8 GPIO

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
D17	GPIO_A_0	I/O CMOS	1.8 V		
E17	GPIO_A_1	I/O CMOS	1.8 V		
F17	GPIO_A_2	I/O CMOS	1.8 V		
G17	GPIO_A_3	I/O CMOS	1.8 V		
H17	GPIO_A_4	I/O CMOS	1.8 V		
J17	GPIO_A_5	I/O CMOS	1.8 V		
K17	GPIO_A_6	I/O CMOS	1.8 V		dual function: SPI_A_CS1#
L17	GPIO_A_7	I/O CMOS	1.8 V		dual function: SPI_B_CS1#
D19	GPIO_B_0	I/O CMOS	1.8 V		
E19	GPIO_B_1	I/O CMOS	1.8 V		
F19	GPIO_B_2	I/O CMOS	1.8 V		
G19	GPIO_B_3	I/O CMOS	1.8 V		
H19	GPIO_B_4	I/O CMOS	1.8 V		
J19	GPIO_B_5	I/O CMOS	1.8 V		
K19	GPIO_B_6	I/O CMOS	1.8 V		
L19	GPIO_B_7	I/O CMOS	1.8 V		
D3	GPIO_C_0	I/O CMOS	1.8 V		
D4	GPIO_C_1	I/O CMOS	1.8 V		
E3	GPIO_C_2	I/O CMOS	1.8 V		
E4	GPIO_C_3	I/O CMOS	1.8 V		
F3	GPIO_C_4	I/O CMOS	1.8 V		dual function: DISP_VDD_EN
F4	GPIO_C_5	I/O CMOS	1.8 V		dual function: DISP_BL_EN
G3	GPIO_C_6	I/O CMOS	1.8 V		dual function: CAM_A_PWR
G4	GPIO_C_7	I/O CMOS	1.8 V		dual function: CAM_A_RST#

Table 10: OSM size-S (GPIO pins)

2.2.9 SDIO

Contact #	Contact Name	I/O Type	I/O Level [5]	PU / PD	Comments
E20	SDIO_A_CMD[1]	I/O CMOS	1.8 V / 3.3 V		command/response port A
F21	SDIO_A_CLK	O CMOS	1.8 V / 3.3 V		clock port A
G20	SDIO_A_D0	I/O CMOS	1.8 V / 3.3 V		data bit 0 port A
G21	SDIO_A_D1	I/O CMOS	1.8 V / 3.3 V		data bit 1 port A
H20	SDIO_A_D2	I/O CMOS	1.8 V / 3.3 V		data bit 2 port A
H21	SDIO_A_D3	I/O CMOS	1.8 V / 3.3 V		data bit 3 port A
J21	SDIO_A_CD#[2]	I OD CMOS	1.8 V / 3.3 V	PU 10k	card-detect port A
D20	SDIO_A_WP[3]	I OD CMOS	1.8 V / 3.3 V	PU 10k	write-protect port A
D21	SDIO_A_PWR_EN[4]	O CMOS	1.8 V / 3.3 V		power enable port A
K21	SDIO_B_CMD[1]	I/O CMOS	1.8 V / 3.3 V		command/response port B
K20	SDIO_B_CLK	O CMOS	1.8 V / 3.3 V		clock port B
L20	SDIO_B_D0	I/O CMOS	1.8 V / 3.3 V		data bit 0 port B
L21	SDIO_B_D1	I/O CMOS	1.8 V / 3.3 V		data bit 1 port B
M21	SDIO_B_D2	I/O CMOS	1.8 V / 3.3 V		data bit 2 port B
N20	SDIO_B_D3	I/O CMOS	1.8 V / 3.3 V		data bit 3 port B
N21	SDIO_B_D4	I/O CMOS	1.8 V / 3.3 V		data bit 4 port B

Contact #	Contact Name	I/O Type	I/O Level [5]	PU / PD	Comments
P20	SDIO_B_D5	I/O CMOS	1.8 V / 3.3 V		data bit 5 port B
P21	SDIO_B_D6	I/O CMOS	1.8 V / 3.3 V		data bit 6 port B
R21	SDIO_B_D7	I/O CMOS	1.8 V / 3.3 V		data bit 7 port B
T21	SDIO_B_CD#[2]	I OD CMOS	1.8 V / 3.3 V	PU 10k	card-detect port B
U20	SDIO_B_WP[3]	I OD CMOS	1.8 V / 3.3 V	PU 10k	write-protect port B
U21	SDIO_B_PWR_EN[4]	O CMOS	1.8 V / 3.3 V		power enable port B

Table 11: OSM size-S (SDIO pins)

[1] The signal is used for card initialization and for command/response transfer. During the initialization, this signal acts as open drain. During the operation, the signal acts in push-pull mode.

[2] This signal indicates when a SD/MMC card is present.

[3] This signal denotes the state of the write-protect tab on SD cards.

[4] This signal enables the power supply for a SD/MMC card device.

[5] The implemented voltage option depends on the specific module. Please refer to the corresponding module documentation.

2.2.10 PWM

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
E18	PWM_0	O CMOS	1.8 V		dual function: DISP_BL_PWM
F18	PWM_1	O CMOS	1.8 V		
G18	PWM_2	O CMOS	1.8 V		
H18	PWM_3	O CMOS	1.8 V		
J18	PWM_4	O CMOS	1.8 V		
K18	PWM_5	O CMOS	1.8 V		

Table 12: OSM size-S (PWM pins)

2.2.11 Analog Signals

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
M18	ADC_0	analog	0 … 1.8 V		
N18	ADC_1	analog	0 … 1.8 V		

Table 13: OSM size-S (ADC pins)

2.2.12 SPI

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
V15	SPI_A_SDO_(IO0)	I/O CMOS	1.8 V		data bit 0 port A
U15	SPI_A_SDI_(IO1)	I/O CMOS	1.8 V		data bit 1 port A
W16	SPI_A_WP_(IO2)	I/O CMOS	1.8 V		data bit 2 port A
W15	SPI_A_HOLD_(IO3)	I/O CMOS	1.8 V		data bit 3 port A
Y15	SPI_A_CS0#	O CMOS	1.8 V		master chip select 0 port A
K17	SPI_A_CS1#	O CMOS	1.8 V		master chip select 1 port A
U16	SPI_A_SCK	O CMOS	1.8 V		clock port A
Y22	SPI_B_SDI	I CMOS	1.8 V		serial data input port B
Y23	SPI_B_SDO	O CMOS	1.8 V		serial data output port B
AA23	SPI_B_CS0#	O CMOS	1.8 V		master chip select 0 port B
L17	SPI_B_CS1#	O CMOS	1.8 V		master chip select 1 port B
Y21	SPI_B_SCK	O CMOS	1.8 V		clock port B

Table 14: OSM size-S (SPI pins)

2.2.13 I2S

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
V21	I2S_A_DATA_IN	I CMOS	1.8 V		audio data input port A
W21	I2S_A_DATA_OUT	O CMOS	1.8 V		audio data output port A
W18	I2S_A_LRCLK[1]	I/O CMOS	1.8 V		left & right synchronization clock port A
W20	I2S_A_BITCLK[1]	I/O CMOS	1.8 V		audio clock port A
V19	I2S_B_DATA_IN	I CMOS	1.8 V		audio data input port B
W19	I2S_B_DATA_OUT	O CMOS	1.8 V		audio data output port A
T18	I2S_B_LRCLK[1]	I/O CMOS	1.8 V		left & right synchronization clock port B
T19	I2S_B_BITCLK[1]	I/O CMOS	1.8 V		audio clock port B
V18	I2S_MCLK	O CMOS	1.8 V		master clock output to I2S codec(s)

Table 15: OSM size-S (I2S pins)

[1] Output, if module acts in Master Mode. Input, if module acts in Slave Mode.

2.2.14 CAN

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
AC17	CAN_A_TX	O CMOS	1.8 V		transmit output port A
AB17	CAN_A_RX	I CMOS	1.8 V		receive input port A
AC19	CAN_B_TX	O CMOS	1.8 V		transmit output port B
AB19	CAN_B_RX	I CMOS	1.8 V		receive input port B

Table 16: OSM size-S (CAN pins)

2.2.15 USB

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
AB13	USB_A_D_N	I/O USB	USB		USB differential data (negative) port A
AC14	USB_A_D_P	I/O USB	USB		USB differential data (positive) port A
AB14	USB_A_ID	I OD CMOS	1.8 V	PU 10k	input to announce an USB 2.0 OTG device on port A
AC15	USB_A_OC#	I OD CMOS	1.8 V	PU 10k	over-current detection port A
AB16	USB_A_VBUS	I USB VBUS	5.0 V		USB VBUS detection port A
AC16	USB_A_EN	O CMOS	1.8 V		power enable for USB VBUS port B
AB23	USB_B_D_N	I/O USB	USB		USB differential data (negative) port B
AC22	USB_B_D_P	I/O USB	USB		USB differential data (positive) port B
AB22	USB_B_ID	I OD CMOS	1.8 V	PU 10k	input to announce an USB 2.0 OTG device on port B
AC21	USB_B_OC#	I OD CMOS	1.8 V	PU 10k	over-current detection port B
AB20	USB_B_VBUS	I USB VBUS	5.0 V		USB VBUS detection port B
AC20	USB_B_EN	O CMOS	1.8 V		power enable for USB VBUS port B
D11	USB_C_D_N	I/O USB	USB		USB differential data (negative) port C
D10	USB_C_D_P	I/O USB	USB		USB differential data (positive) port C
D9	USB_C_ID	I OD CMOS	1.8 V	PU 10k	input to announce an USB 2.0 OTG device on port C
C8	USB_C_OC#	I OD CMOS	1.8 V	PU 10k	over-current detection port C
C9	USB_C_VBUS	I USB VBUS	5.0 V		USB VBUS detection port C
C10	USB_C_EN	O CMOS	1.8 V		power enable for USB VBUS port C
A9	USB_C_SSTX_N[1]	O USB SS	USB SS		SuperSpeed transmit data (negative) port C
A8	USB_C_SSTX_P[1]	O USB SS	USB SS		SuperSpeed transmit data (positive) port C

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
B11	USB_C_SSRX_N[1]	I USB SS	USB SS		SuperSpeed receive data (negative) port C
B10	USB_C_SSRX_P[1]	I USB SS	USB SS		SuperSpeed receive data (positive) port C

Table 17: OSM size-S (USB pins)

[1] AC coupled on carrier.

2.2.16 I2C

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
AA15	I2C_A_SCL	I/O OD CMOS	1.8 V	PU 2k2	clock signal port A
AA16	I2C_A_SDA	I/O OD CMOS	1.8 V	PU 2k2	data signal port A
AA20	I2C_B_SCL	I/O OD CMOS	1.8 V	PU 2k2	clock signal port B
AA21	I2C_B_SDA	I/O OD CMOS	1.8 V	PU 2k2	data signal port B

Table 18: OSM size-S (I2C pins)

2.2.17 PCIe

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
AB1	PCIe_A_HSI0_P[1]	I PCIe	PCIe		receive data (positive)
AB2	PCIe_A_HSI0_N[1]	I PCIe	PCIe		receive data (negative)
AC2	PCIe_A_HSO0_P[1]	O PCIe	PCIe		transmit data (positive)
AC3	PCIe_A_HSO0_N[1]	O PCIe	PCIe		transmit data (negative)
W2	PCIe_CLKREQ#	I OD CMOS	1.8 V	PU 10k	request reference clock
V2	PCIe_A_PERST#	O CMOS	1.8 V		port reset
W1	PCIe_REFCLK_P	O PCIe	PCIe		reference clock (positive)
Y1	PCIe_REFCLK_N	O PCIe	PCIe		reference clock (negative)
T2	PCIe_WAKE#	I OD CMOS	1.8 V	PU 10k	wake up interrupt to host
U1	PCIe_SMDAT	I/O OD CMOS	1.8 V	PU 2k2	system management bus I2C data
T1	PCIe_SMCLK	O OD CMOS	1.8 V	PU 2k2	system management bus I2C clock
R2	PCIe_SM_ALERT#	I OD CMOS	1.8 V	PU 2k2	system management bus interrupt signal

Table 19: OSM size-S (PCIe pins)

[1] AC coupled on carrier.

2.2.18 MIPI CSI

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
C1	CSI_A_DATA0_N	I MIPI CSI			data 0 (negative)
B1	CSI_A_DATA0_P	I MIPI CSI			data 0 (positive)
A2	CSI_A_DATA1_N	I MIPI CSI			data 1 (negative)
A3	CSI_A_DATA1_P	I MIPI CSI			data 1 (positive)
A5	CSI_A_DATA2_N	I MIPI CSI			data 2 (negative)
A6	CSI_A_DATA2_P	I MIPI CSI			data 2 (positive)
B6	CSI_A_DATA3_N	I MIPI CSI			data 3 (negative)
B7	CSI_A_DATA3_P	I MIPI CSI			data 3 (positive)
B3	CSI_A_CLOCK_N	I MIPI CSI			clock (negative)
B4	CSI_A_CLOCK_P	I MIPI CSI			clock (positive)
C2	CAM_MCK	O CMOS	1.8 V		master clock
C3	CAM_A_SDA CSI_A_TX_N	I/O OD CMOS O MIPI CSI	1.8 V	PU 2k2	camera data support link I2C data (CSI 2.0) transmit data (negative) (CSI 3.0)

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
C4	CAM_A_SCL CSI_A_TX_P	I/O OD CMOS O MIPI CSI	1.8 V	PU 2k2	camera data support link I2C clock (CSI 2.0) transmit data (positive) (CSI 3.0)
G3	CAM_A_PWR	O CMOS	1.8 V		camera power enable dual function: GPIO_C_6
G4	CAM_A_RST#	O CMOS	1.8 V		camera reset dual function: GPIO_C_7

Table 20: OSM size-S (MIPI CSI pins)

2.2.19 Display

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
AB11	DSI_DATA0_N LVDS_A_LANE0_N	O MIPI DSI O LVDS			data 0 (negative)
AB10	DSI_DATA0_P LVDS_A_LANE0_P	O MIPI DSI O LVDS			data 0 (positive)
AC9	DSI_DATA1_N LVDS_A_LANE1_N	O MIPI DSI O LVDS			data 1 (negative)
AC8	DSI_DATA1_P LVDS_A_LANE1_P	O MIPI DSI O LVDS			data 1 (positive)
AC6	DSI_DATA2_N LVDS_A_LANE2_N	O MIPI DSI O LVDS			data 2 (negative)
AC5	DSI_DATA2_P LVDS_A_LANE2_P	O MIPI DSI O LVDS			data 2 (positive)
AB5	DSI_DATA3_N LVDS_A_LANE3_N	O MIPI DSI O LVDS			data 3 (negative)
AB4	DSI_DATA3_P LVDS_A_LANE3_P	O MIPI DSI O LVDS			data 3 (positive)
AB8	DSI_CLOCK_N LVDS_A_CLK_N	O MIPI DSI O LVDS			clock (negative)
AB7	DSI_ CLOCK _P LVDS_A_CLK_P	O MIPI DSI O LVDS			clock (positive)
AA3	DSI_TE	I CMOS	1.8 V		DSI panel tearing effect signal, LVDS: n.u.
F3	DISP_VDD_EN	O CMOS	1.8 V		primary display power enable dual function: GPIO_C_4
F4	DISP_BL_EN	O CMOS	1.8 V		primary display backlight enable dual function: GPIO_C_5
E18	DISP_BL_PWM	O CMOS	1.8 V		primary display brightness control dual function: PWM_0
Y7	RGB_R0	O CMOS	3.3 V		red data bit 0
AA6	RGB_R1	O CMOS	3.3 V		red data bit 1
Y6	RGB_R2	O CMOS	3.3 V		red data bit 2
AA5	RGB_R3	O CMOS	3.3 V		red data bit 3
Y5	RGB_R4	O CMOS	3.3 V		red data bit 4
Y4	RGB_R5	O CMOS	3.3 V		red data bit 5
W4	RGB_G0	O CMOS	3.3 V		green data bit 0
V3	RGB_G1	O CMOS	3.3 V		green data bit 1
V4	RGB_G2	O CMOS	3.3 V		green data bit 2
U3	RGB_G3	O CMOS	3.3 V		green data bit 3

Contact #	Contact Name	I/O Type	I/O Level	PU / PD	Comments
T3	RGB_G4	O CMOS	3.3 V		green data bit 4
T4	RGB_G5	O CMOS	3.3 V		green data bit 5
R4	RGB_B0	O CMOS	3.3 V		blue data bit 0
R3	RGB_B1	O CMOS	3.3 V		blue data bit 1
P3	RGB_B2	O CMOS	3.3 V		blue data bit 2
N3	RGB_B3	O CMOS	3.3 V		blue data bit 3
N4	RGB_B4	O CMOS	3.3 V		blue data bit 4
M3	RGB_B5	O CMOS	3.3 V		blue data bit 5
M4	RGB_(PIXEL)CLK	O CMOS	3.3 V		pixel clock
L3	RGB_VSYNC	O CMOS	3.3 V		vertical SYNC
K3	RGB_HSYNC	O CMOS	3.3 V		horizontal SYNC
K4	RGB_DISP	O CMOS	3.3 V		display ON/OFF
J4	RGB_DE	O CMOS	3.3 V		data enable
J3	RGB_RESET#	O CMOS	3.3 V		global reset
H3	RGB_CS#	O CMOS	3.3 V		chip select

Table 21: OSM size-S (DISP pins)

3 Handling

3.1 Packaging

The OSM modules are shipped in trays. One tray can hold 24 modules. An empty tray is used as top cover.

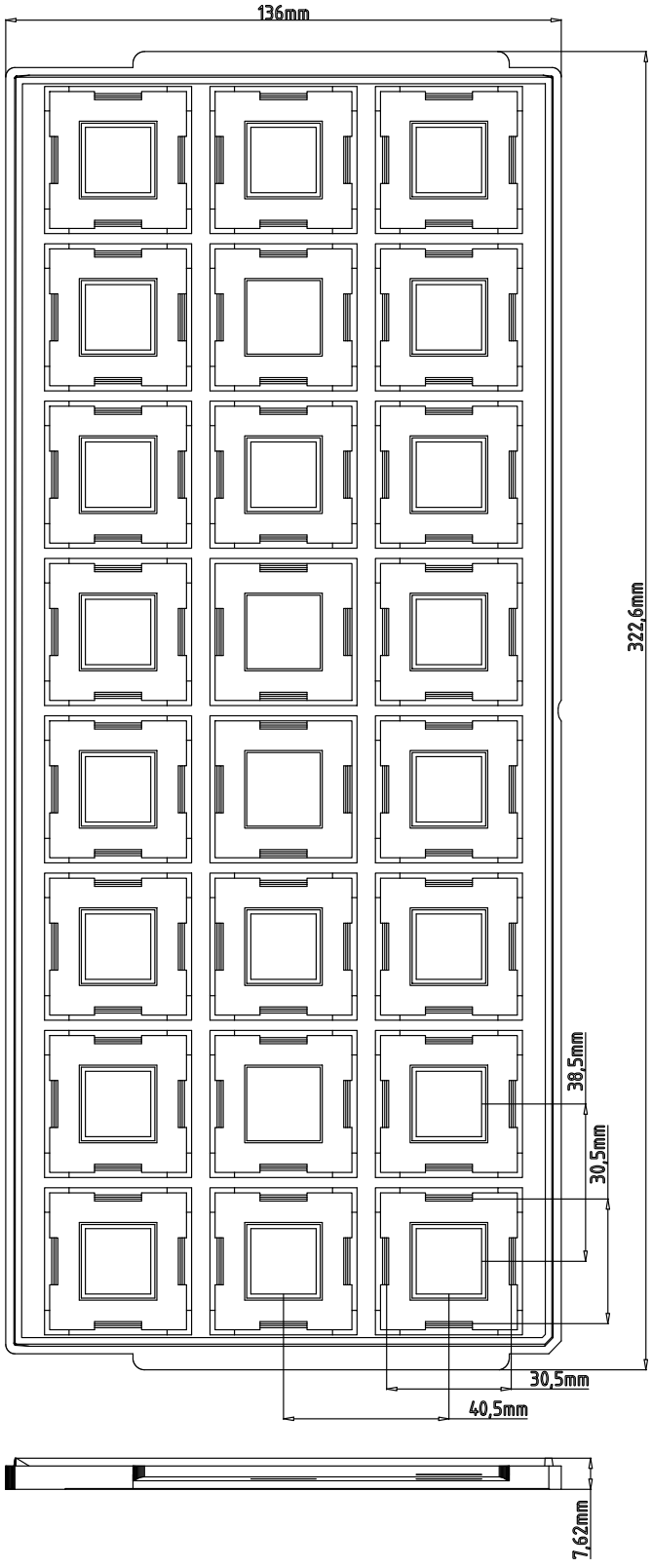


Figure 4: Shipping Tray

Please note that the trays are on loan only and must be returned to F&S after use.

3.2 Identification

3.2.1 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker which includes the serial number. Enter your serial number here: https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 5: Matrix Code Sticker (example)

3.2.2 PCB Information

Due to the lack of space, the pcb information

- name & revision (etch)
- UL marking, batch & date code (soldermask)

are only available in a readable format on the BOT side of the pcb. The following picture shows the marking positions.

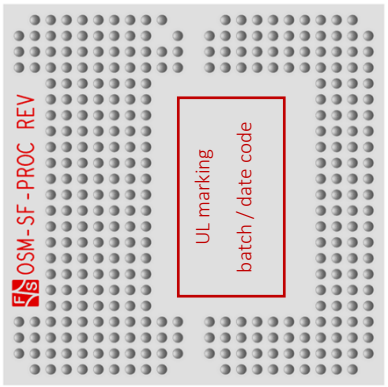


Figure 6: F&S OSM Size-S (pcb information, BOT view)

3.3 Production

3.3.1 Recommended Stencil Parameters for Soldering

For the processing of both (LGA and FTGA variants of the modules) we recommend the following stencil and solder paste configuration:

Parameter	Recommendation
Stencil Thickness	100 µm
Material	Laser-cut, electropolished stainless steel (optional nano-coating)
Aperture Size (pad Ø: 0,80 mm)	0,80 mm (same as pad)
Aspect Ratio	8,0 (minimum requirement ≥ 1,5)
Area Ratio	2,0 (minimum requirement ≥ 0,66)
Solder Paste	SAC305 minimum Type 4
Flux	No-clean
SPI Target Volume	0,050 mm³ ± 15 %
SPI Target Height	95 µm - 120 µm

Table 22: Stencil & Solder Paste Configuration

3.3.2 Orientation Mark for Placement

For an optical inspection of the correct orientation of the module during the placement on the carrier one can use the F&S-logo on TOP side as an orientation mark. The following picture shows the position of the logo in relation to the contact grid, which is the same for all F&S OSM modules (size-S).

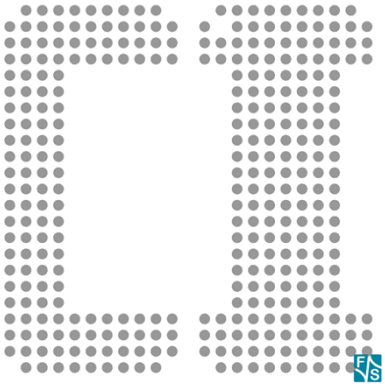


Figure 7: F&S OSM Size-S (F&S logo as orientation mark, TOP view through the board)

3.3.3 Pick & Place Recommendation

To ensure reliable SMT placement[1] of the modules, we recommend the following pick positions depending on module type and assembly constraints:

First Pick Position (recommended)

- Center of Processor Package
- applicable for all modules unless the SoC has an uneven surface

Secondary Pick Position (alternative)

- Top Center of the eMMC Flash Chip
- use if the processor package surface is not flat enough to allow reliable vacuum pickup

Both positions are shown in the figure below (FS 8ULP-OSM-SF):

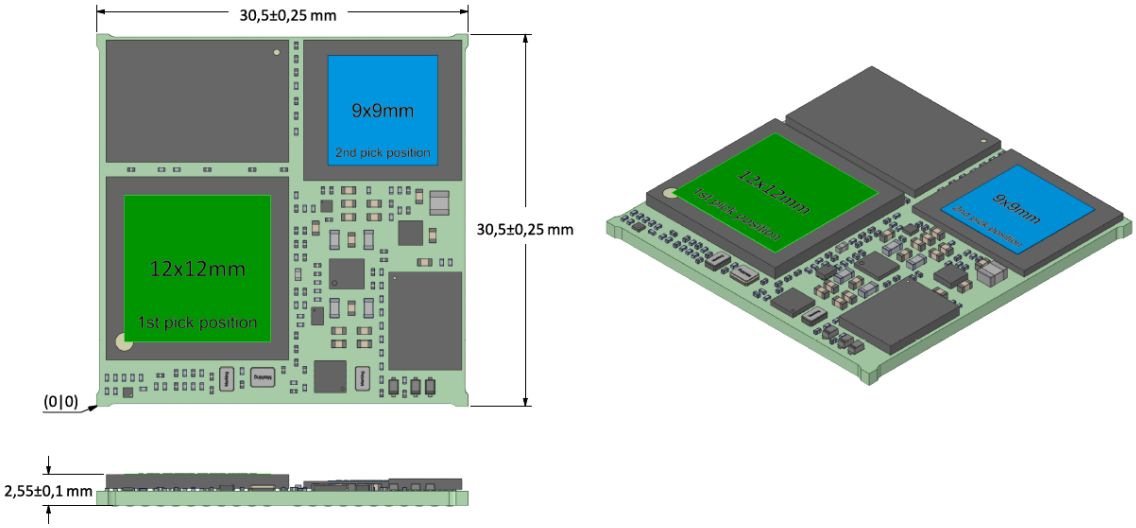


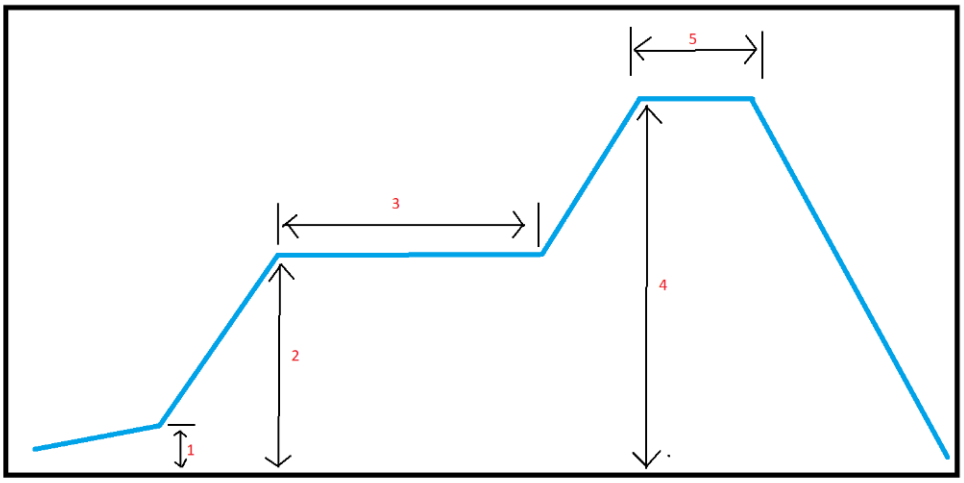
Figure 8: F&S OSM Size-S (recommended pick positions)

[1] Both, round and rectangular vacuum tip shapes are suitable.

3.3.4 Soldering Profile

As the exact soldering profile depends on many factors, the following information are to understand as an initial reference[1].
Preconditions:

- Dry OSM module (MSL 3).
- Only 2 soldering cycles are permitted in total.



		min	typ	max
1	SYNC for temperature-equalization (if required)			80 °C[2]
2	Preheat (Temperature)		160 °C	190 °C
3	Preheat (Time)		≤ 60 s	90 s
4	Soldering (Temperature)	225 °C[3]		240 °C
5	Soldering (Time @ 240 °C)		15 s	30 s

Figure 9: Soldering Profile (Vapor phase, example)

[1] The profile is only valid for Vapor Phase-Soldering. Reflow may require higher temperatures. **260 °C must not be exceeded.**

[2] The total time above 60 °C must not exceed 600 s.

[3] FTGA

4 Appendix

4.1 Second source rules

The qualifications of products from a second source are done autonomously by F&S. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible. F&S does not use broker components without the consent of the customer.

4.2 RoHS and REACH statement

Please see the following webpage: https://www.fs-net.de/en/support/certifications/

4.3 Important Notice

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